1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J110 MLB SCHEMATIC

09/25/14

Page	(.csa)	Contents	Sync	Date
1	1	Table of Contents	MASTER	MASTER
2	2	BOM Configuration	J43_MLB	01/17/2013
3	3	BOM Variants	MASTER	MASTER
4	4	PD Parts	MASTER	MASTER
5	5	CPU GFX/NCTF/RSVD	WILL_J43	09/13/2012
6	6	CPU Misc/JTAG/CFG/RSVD	WILL_J43	09/13/2012
7	7	CPU DDR3/LPDDR3 Interfaces	WILL_J43	09/13/2012
8	8	CPU/PCH POWER	J43_MLB	10/02/2012
9	9	CPU/PCH GROUNDS	J43_MLB	10/02/2012
10	10	CPU Decoupling	LABEL_J41	01/11/2013
11	12	PCH Decoupling	WILL_J43	09/13/2012
12	13	PCH Audio/JTAG/SATA/CLK	WILL_J43	12/17/2012
13	14	PCH PM/PCI/GFX	J43_MLB	02/20/2013
14	15	PCH PCIe/USB/LPC/SPI/SMBus	WILL_J43	09/13/2012
15	16	PCH GPIO/MISC/LPIO	WILL_J43	01/14/2013
16	18	CPU/PCH Merged XDP	WILL_J43	12/17/2012
17	19	Chipset Support	J43_MLB1	01/09/2013
18	20	Project Chipset Support	J43_MLB	01/17/2013
19	22	DDR3 VREF MARGINING	WILL_J43	02/04/2013
20	23	LPDDR3 DRAM Channel A (0-31)	MASTER	MASTER
21	24	LPDDR3 DRAM Channel A (32-63)	MASTER	MASTER
22	25	LPDDR3 DRAM Channel B (0-31)	MASTER	MASTER
23	26	LPDDR3 DRAM Channel B (32-63)	MASTER	MASTER
24	27	LPDDR3 DRAM Termination	J43_MLB	09/21/2012
25	28	Thunderbolt Host (1 of 2)	T29_RR	01/19/2013
26	29	Thunderbolt Host (2 of 2)	T29_RR	12/17/2012
27	30	TBT Power Support	WILL_J43	12/17/2012
28	32	Thunderbolt Connector A	T29_RR	10/26/2012
29	35	Wireless Connector	J43_MLB	10/02/2012
30	37	SSD Connector	J43_MLB	02/20/2013
31	39	Camera 1 of 2	J43_MLB1	01/09/2013
32	40	Camera 2 of 2	J43_MLB	09/14/2012
33	46	External A USB3 Connector	J43_MLB	02/20/2013
34	48	IPD Connector	J43_MLB	01/17/2013
35	50	SMC	WILL_J43	12/17/2012

Page	(.csa)	Contents	Sync	Date
36	51	SMC Shared Support	WILL_J43	12/17/2012
37	52	SMC Project Support	J43_MLB	02/20/2013
38	53	SMBus Connections	J43_MLB	09/28/2012
39	54	High Side Current Sensing	SID_J41	02/26/2013
40	55	Voltage & Load Side Current Sensing	SID_J41	02/26/2013
41	56	Debug Sensors 1	SID_J41	02/26/2013
42	58	Thermal Sensors	J43_MLB	02/20/2013
43	60	Fan	J43_MLB	09/13/2012
44	61	SPI Debug Connector	YHARTANTO_J44	01/09/2013
45	64	Audio: Speaker Amp	J43_MLB	09/04/2012
46	69	Battery Connector & Hall Effect	MASTER	MASTER
47	70	DC-In & G3H Supply	J43_MLB	09/13/2012
48	71	PBus Supply & Battery Charger	J43_MLB	09/14/2012
49	72	CPU VR12.6 VCC Regulator IC	J43_MLB	10/09/2012
50	73	CPU VR12.5 VCC Power Stage	J43_MLB	09/21/2012
51	74	LPDDR3 Supply	J43_MLB	09/17/2012
52	75	5V S4RS3 / 3.3V S5 Power Supply	J43_MLB	10/02/2012
53	76	1.05V S0 Power Supply	J43_MLB	09/10/2012
54	77	LCD/KBD Backlight Driver	J43_MLB	09/13/2012
55	78	Misc Power Supplies	J43_MLB	10/04/2012
56	80	Power FETs	J43_MLB	10/04/2012
57	81	Power Control	J43_MLB	09/16/2012
58	83	Internal DisplayPort Connector	J43_MLB	09/11/2012
59	95	LIO Connector	CLEAN_J41	11/13/2012
60	100	Power Aliases	WILL_J43	12/17/2012
61	102	Signal Aliases	MASTER	MASTER
62	104	Func Test / No Test	WILL_J43	12/17/2012
63	105	Project FCT/NC/Aliases	MASTER	MASTER
64	110	PCB Rule Definitions	J43_MLB	10/24/2012
65	111	CPU Constraints	J43_MLB	09/21/2012
66	112	PCH Constraints 1	CLEAN_J41	11/13/2012
67	113	PCH Constraints 2	J43_MLB	09/14/2012
68	114	Memory Constraints	CHINMAY_J41	09/07/2012
69	115	Thunderbolt Constraints	CHINMAY_J41	09/07/2012
70	116	Camera Constraints	CHINMAY_J41	09/07/2012
71	117	SMC Constraints	CHINMAY_J41	09/13/2012
72	118	Project Specific Constraints	J43_MLB	09/13/2012
73	120	Reference	MASTER	MASTER

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00384	1	SCHEM,MLB,J110	SCH	CRITICAL	
820-00164	1	PCBF,MLB,J110	PCB	CRITICAL	

DRAWING
TITLE=MLB
AGENCY=DRAWING
LAST_MODIFIED=Thu Sep 25 16:36:28 2014

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE
<PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 1 OF 120
SHEET 1 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:PVT,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TBTHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS,SSD_LPSR:S3
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	XDP,SAMCONN
MLB_DEBUG:PVT	BKLT:PROD,XDP,SAMCONN,ISNS:ENG,DBGLED,XDP_CONN
MLB_DEBUG:PROD	BKLT:PROD,SAMCONN,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,PSVGS_ISNS:YES,A3PORT_ISNS:YES,SSD_ISNS:YES,LCDBKLT_ISNS:YES,P3V3SS_ISNS:YES,3VSSB_ISNS:YES,OTHER_HS_ISNS:YES,CAM_ISNS:YES,CPUDDR_ISNS:YES,PANEL_ISNS:YES
ISNS:PROD	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,PSVGS_ISNS:NO,A3PORT_ISNS:NO,SSD_ISNS:YES,LCDBKLT_ISNS:NO,P3V3SS_ISNS:NO,3VSSB_ISNS:NO,OTHER_HS_ISNS:NO,CAM_ISNS:NO,CPUDDR_ISNS:NO,PANEL_ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:MICRON_8GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:MICRON_8GB
DDR3:HYNIX_16GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_16GB
DDR3:SAMSUNG_16GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:SAMSUNG_16GB
DDR3:ELPIDA_16GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_16GB
DDR3:MICRON_16GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:MICRON_16GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
4GB	0	0
8GB	0	1
16GB	1	0
RSVD	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	20MHz Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sensa R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S00014	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
870-5074	870-1938		ALL	ALT POGO PIN W_O CAP
870-5071	870-1940		ALL	ALT POGO PIN W_O CAP
860-3428	860-1327		ALL	ALT STANDOFF W_O MYLAR
860-3690	860-1328		ALL	ALT STANDOFF W_O MYLAR
333S0787	333S0677	DRAM_TYPE:HYNIX_4GB	ALL	ALT STANDOFF W_O MYLAR
333S0785	333S0681	DRAM_TYPE:HYNIX_8GB	ALL	ALT STANDOFF W_O MYLAR

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0915	1	EEPROM,4MBIT,SPI,50MHZ,1.8V,USON8	U2890	CRITICAL	TBTROM:BLANK
341S00159	1	T29,EEPROM,FALCON RIDGE(V27.1), PROto 0,J110/J113	U2890	CRITICAL	TBTROM:PROG
338S1214	1	IC,SMC12-B1,40MHZ/500MIPS MCU,157BGA	U5000	CRITICAL	SMC:BLANK
335S00006	1	IC,SERIAL FLASH,64 MBIT 3V,WSON,QE=1	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S00007	1	IC,SERIAL FLASH,64 MBIT 3V,WSON,QE=1	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S00153	1	IC,EFI ROM(V8108), PROTO 0,J110/J113	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00029	1	BDW,QGH9,D0,1.8,15W,2+2,0.7,4M,B1168	U0500	CRITICAL	CPU:2.1GHZ
337S00073	1	BDW,QGHB,D0,1.6,15W,2+2,0.6,4M,B1168	U0500	CRITICAL	CPU:1.6GHZ
338S00069	1	IC,TBT,FR-2C,288, 12X12 FC-CSP,TRAY	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2KFEB4G,S2 CMRA,8X8,208FCBGA	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J110_MLB
946-5477	1	UV GLUE,MLB,J41_J43	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S00036	2	MOSFET,N-CH,25V,30A,9.6M,BP 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S00037	2	MOSFET,N-CH,25V,30A,6.1M,BP 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1194	2	MOSFET,N-CH,30V,15.3A,12M,BP 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET,N-CH,30V,22A,6.0M,BP 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	
825-7987	1	LABEL,MLB,J41/J43	NEW_LABEL		

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S00001	4	IC,SDRAM,23NM,8GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S00003	4	IC,SDRAM,23NM,16GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0793	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0791	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0793	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0791	4	IC,SDRAM,16GB,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_8GB
333S0789	4	IC,SDRAM,25nm,32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_16GB

SYNC MASTER=J43_MLB SYNC DATE=01/17/2013

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 2 OF 120
SHEET 2 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00613	PCBA,MLB,BETTER,HY-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_4GB,ALTERNATE
639-00614	PCBA,MLB,BETTER,HY-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_8GB,ALTERNATE
639-00616	PCBA,MLB,BETTER,SM-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_4GB,ALTERNATE
639-00617	PCBA,MLB,BETTER,SM-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_8GB,ALTERNATE
639-00621	PCBA,MLB,BETTER,EL-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_4GB
639-00622	PCBA,MLB,BETTER,EL-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_8GB
639-00695	PCBA,MLB,BETTER,EL-16GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_16GB
685-00043	CMN PTS,PCBA,MLB,X430	MLB_COMMON,J110_MLB
685-00044	VCORE FET,REN,X430	VCORE_FET:REN
685-00045	VCORE FET,VSHY,X430	VCORE_FET:VSHY

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00044	685-00045		ALL	Renesas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00147	1	IC,SMC-A3,EXT,Vxxxx,PROTO 0,J110	U5000	CRITICAL	SMC:PROG

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00043	1	CMN PTS,PCBA,MLB,J110	CMNPTS	CRITICAL	MLB_CMNPTS
685-00045	1	VCORE FET,VSHY,J110	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
BOM Variants

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 3 OF 120

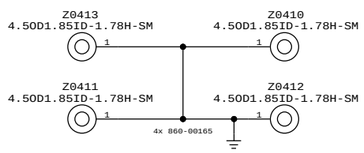
SHEET 3 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

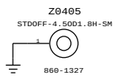
PD Module Parts

806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

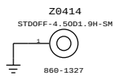
CPU Heat Sink Mounting Bosses



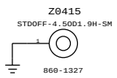
Fan Boss



X21 Boss

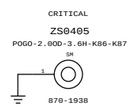


SSD Boss

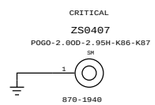


EMI I/O Pogo Pins

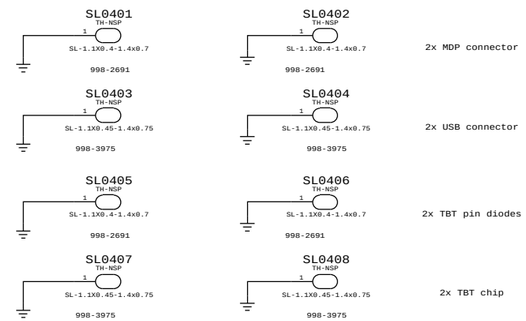
DisplayPort Pogo



USB/SD Card Pogo



Can Slots



SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE

PD Parts

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

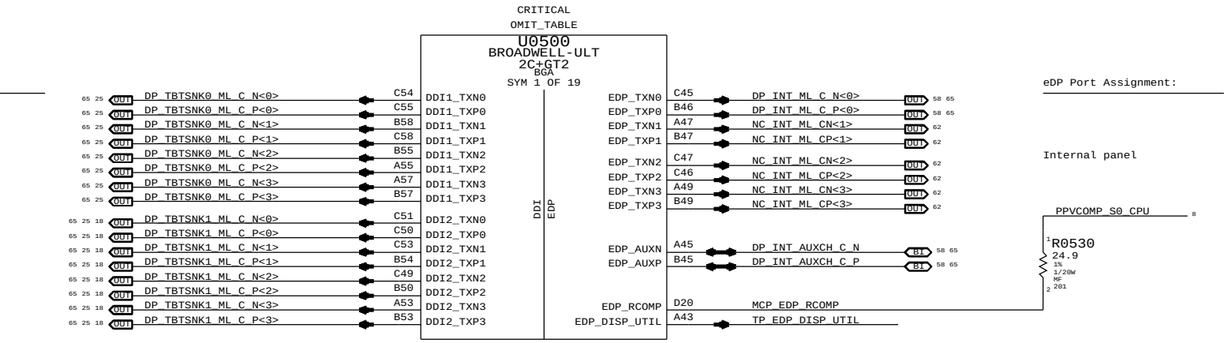
REVISION <E4LABEL>

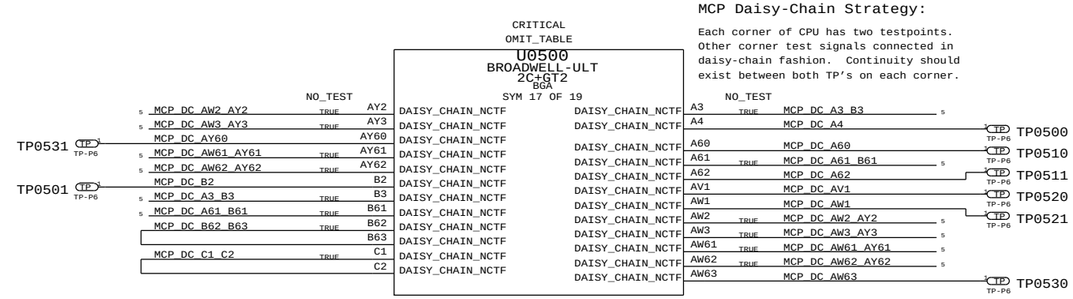
BRANCH <BRANCH>

PAGE 4 OF 120

SHEET 4 OF 73

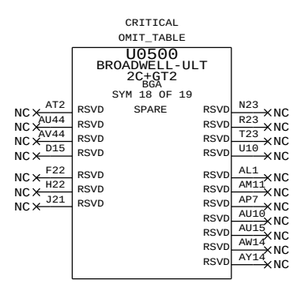
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





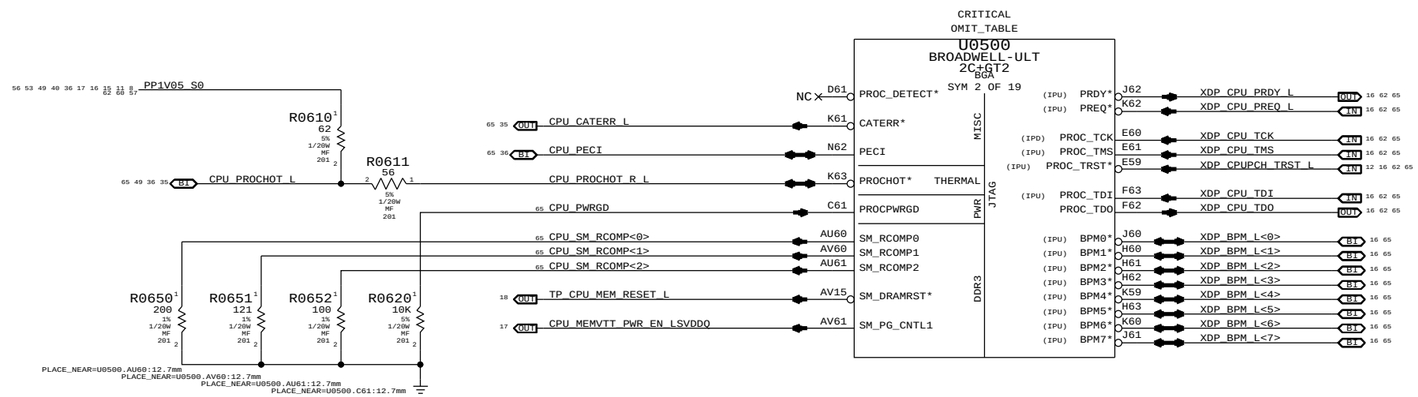
MCP Daisy-Chain Strategy:

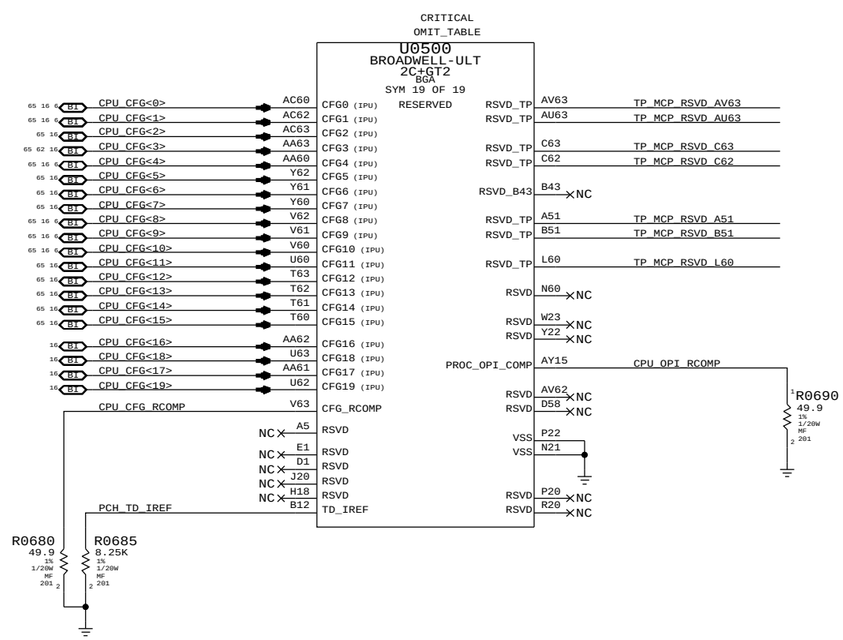
Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.



SYNC MASTER=WILL J43	SYNC DATE=09/13/2012
PAGE TITLE	CPU GFX/NCTF/RSVD
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 5 OF 120
	SHEET 5 OF 73

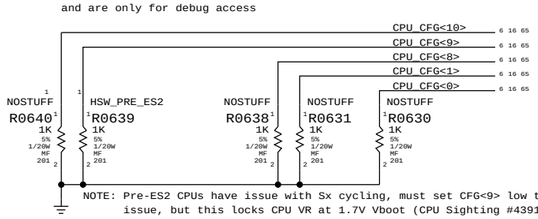
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



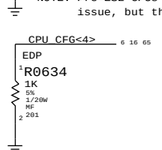


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC MASTER=WILL_J43 SYNC DATE=09/13/2012

PAGE TITLE

CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

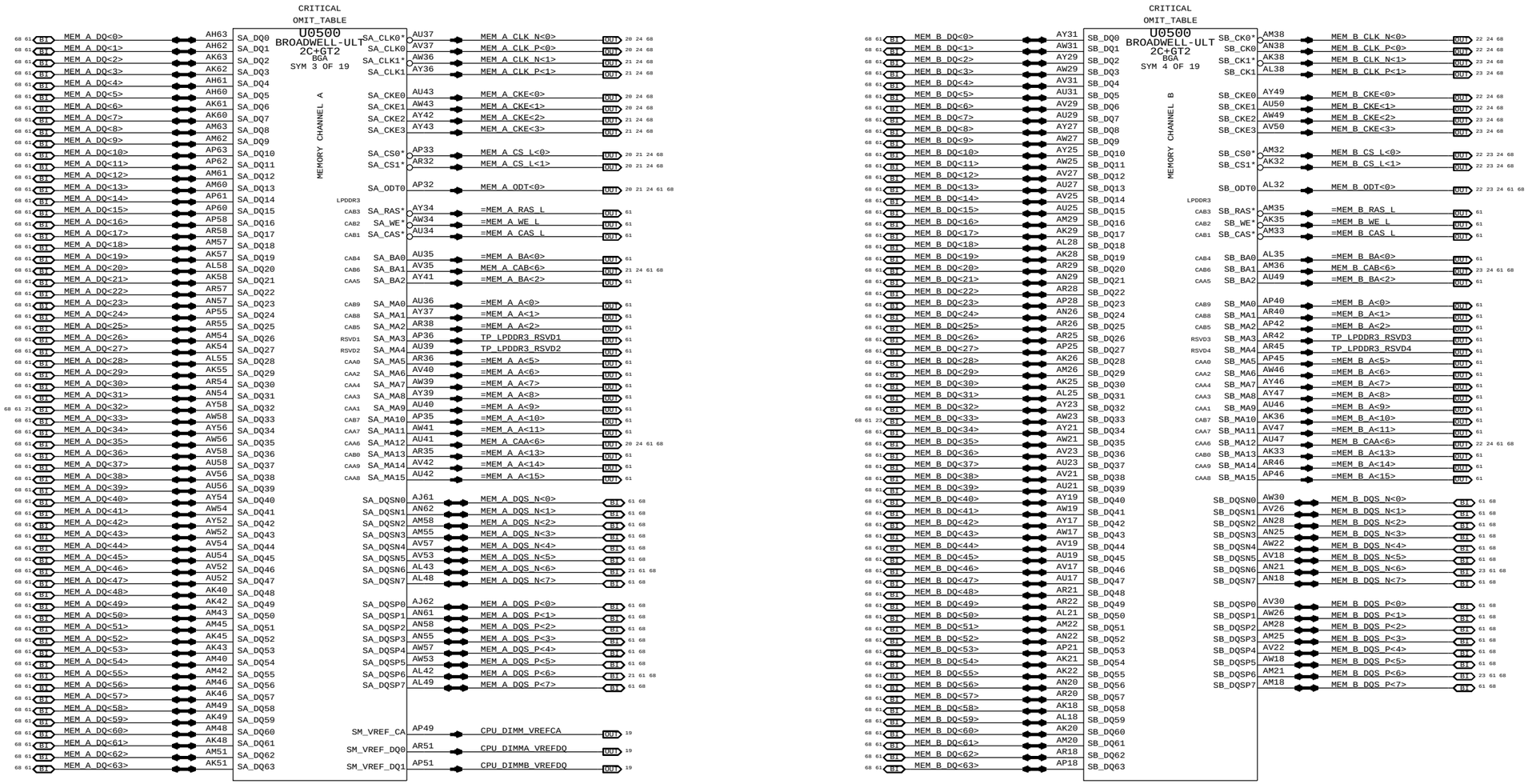
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 6 OF 120

SHEET 6 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

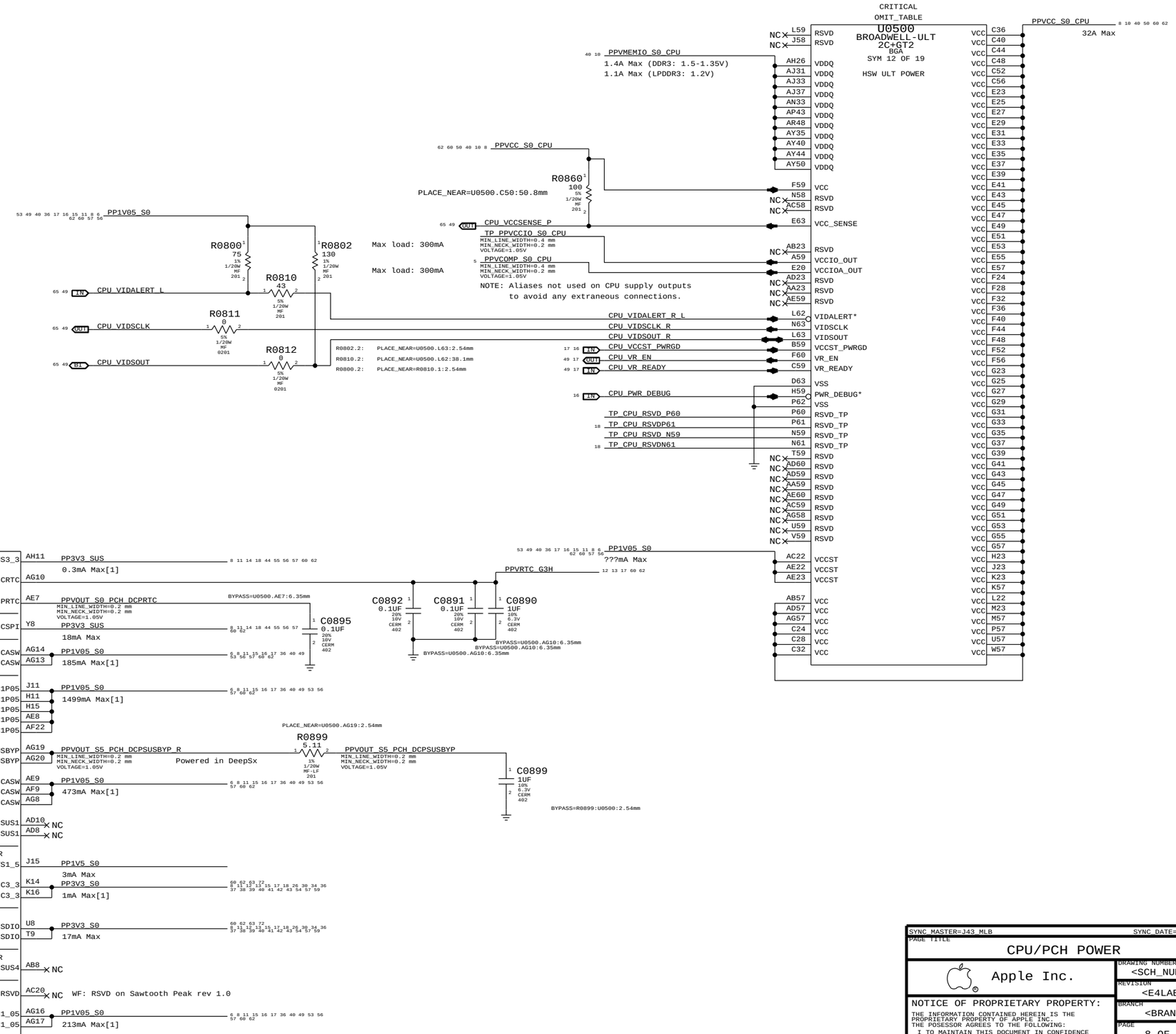
BRANCH <BRANCH>

PAGE 7 OF 120

SHEET 7 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH POWER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 8 OF 120
SHEET 8 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS	VSS	V58
G5	VSS	VSS	AH46
G6	VSS	VSS	V23
G8	VSS	VSS	E62
H13	VSS	VSS	AH16

VSS_SENSE

CPU_VCCSENSE_N — OUT — 49 65

R0960
100
5%
1/20W
MF
201

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 9 OF 120
SHEET 9 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

62 60 50 40 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402	NO STUFF C1001 10UF 20% 4V X6S 0402	NO STUFF C1002 10UF 20% 4V X6S 0402	NO STUFF C1003 10UF 20% 4V X6S 0402	NO STUFF C1004 10UF 20% 4V X6S 0402	NO STUFF C1005 10UF 20% 4V X6S 0402	NO STUFF C1006 10UF 20% 4V X6S 0402	NO STUFF C1007 10UF 20% 4V X6S 0402	NO STUFF C1008 10UF 20% 4V X6S 0402	NO STUFF C1009 10UF 20% 4V X6S 0402	NO STUFF C1010 10UF 20% 4V X6S 0402	NO STUFF C1011 10UF 20% 4V X6S 0402	NO STUFF C1012 10UF 20% 4V X6S 0402	NO STUFF C1013 10UF 20% 4V X6S 0402	NO STUFF C1014 10UF 20% 4V X6S 0402	NO STUFF C105A 10UF 20% 4V X6S 0402	CRITICAL C105B 10UF 20% 4V X6S 0402	CRITICAL C105C 10UF 20% 4V X6S 0402	NO STUFF C105D 10UF 20% 4V X6S 0402	NO STUFF C105E 10UF 20% 4V X6S 0402	CRITICAL C105F 10UF 20% 4V X6S 0402		
NO STUFF C1015 10UF 20% 4V X6S 0402	NO STUFF C1016 10UF 20% 4V X6S 0402	NO STUFF C1017 10UF 20% 4V X6S 0402	NO STUFF C1018 10UF 20% 4V X6S 0402	NO STUFF C1019 10UF 20% 4V X6S 0402	NO STUFF C1020 10UF 20% 4V X6S 0402	NO STUFF C1021 10UF 20% 4V X6S 0402	NO STUFF C1030 10UF 20% 4V X6S 0402	NO STUFF C104A 10UF 20% 4V X6S 0402	NO STUFF C104B 10UF 20% 4V X6S 0402	NO STUFF C104C 10UF 20% 4V X6S 0402	CRITICAL C104D 10UF 20% 4V X6S 0402	NO STUFF C104E 10UF 20% 4V X6S 0402	CRITICAL C104F 10UF 20% 4V X6S 0402	CRITICAL C106A 10UF 20% 4V X6S 0402	NO STUFF C106B 10UF 20% 4V X6S 0402	NO STUFF C106C 10UF 20% 4V X6S 0402	NO STUFF C106D 10UF 20% 4V X6S 0402	NO STUFF C106E 10UF 20% 4V X6S 0402			
CRITICAL C1070 10UF 20% 4V X6S 0402	CRITICAL C1071 10UF 20% 4V X6S 0402	NO STUFF C1072 10UF 20% 4V X6S 0402	NO STUFF C1073 10UF 20% 4V X6S 0402	NO STUFF C1074 10UF 20% 4V X6S 0402	NO STUFF C1075 10UF 20% 4V X6S 0402	CRITICAL C1076 10UF 20% 4V X6S 0402	CRITICAL C1077 10UF 20% 4V X6S 0402	NO STUFF C1078 10UF 20% 4V X6S 0402	NO STUFF C1079 10UF 20% 4V X6S 0402	NO STUFF C1080 10UF 20% 4V X6S 0402	NO STUFF C1081 10UF 20% 4V X6S 0402	NO STUFF C1082 10UF 20% 4V X6S 0402	CRITICAL C1083 10UF 20% 4V X6S 0402	CRITICAL C1084 10UF 20% 4V X6S 0402							
CRITICAL C1085 10UF 20% 4V X6S 0402	CRITICAL C1086 10UF 20% 4V X6S 0402	CRITICAL C1087 10UF 20% 4V X6S 0402	NO STUFF C1088 10UF 20% 4V X6S 0402	NO STUFF C1089 10UF 20% 4V X6S 0402	NO STUFF C1090 10UF 20% 4V X6S 0402	CRITICAL C1091 10UF 20% 4V X6S 0402	CRITICAL C1092 10UF 20% 4V X6S 0402	NO STUFF C1093 10UF 20% 4V X6S 0402	NO STUFF C1094 10UF 20% 4V X6S 0402	NO STUFF C1095 10UF 20% 4V X6S 0402	NO STUFF C1096 10UF 20% 4V X6S 0402	CRITICAL C1097 10UF 20% 4V X6S 0402									
NO STUFF C1022 10UF 20% 4V X6S 0402	NO STUFF C1023 10UF 20% 4V X6S 0402	NO STUFF C1024 10UF 20% 4V X6S 0402	NO STUFF C1025 10UF 20% 4V X6S 0402	NO STUFF C1026 10UF 20% 4V X6S 0402	NO STUFF C1027 10UF 20% 4V X6S 0402	NO STUFF C1028 10UF 20% 4V X6S 0402	NO STUFF C1029 10UF 20% 4V X6S 0402	NO STUFF C1032 10UF 20% 4V X6S 0402	NO STUFF C1033 10UF 20% 4V X6S 0402	NO STUFF C1034 10UF 20% 4V X6S 0402	NO STUFF C1035 10UF 20% 4V X6S 0402	NO STUFF C1036 10UF 20% 4V X6S 0402	NO STUFF C1037 10UF 20% 4V X6S 0402	NO STUFF C1038 10UF 20% 4V X6S 0402							
NO STUFF C1039 10UF 20% 4V X6S 0402	NO STUFF C1044 10UF 20% 4V X6S 0402	NO STUFF C1045 10UF 20% 4V X6S 0402	NO STUFF C1046 10UF 20% 4V X6S 0402	NO STUFF C1047 10UF 20% 4V X6S 0402	NO STUFF C1048 10UF 20% 4V X6S 0402	NO STUFF C1049 10UF 20% 4V X6S 0402															
NO STUFF C1056 10UF 20% 4V X6S 0402	NO STUFF C1057 10UF 20% 4V X6S 0402	NO STUFF C1058 10UF 20% 4V X6S 0402	NO STUFF C1059 10UF 20% 4V X6S 0402	NO STUFF C1062 10UF 20% 4V X6S 0402	NO STUFF C1063 10UF 20% 4V X6S 0402	NO STUFF C1064 10UF 20% 4V X6S 0402	NO STUFF C1065 10UF 20% 4V X6S 0402	NO STUFF C1066 10UF 20% 4V X6S 0402	NO STUFF C1067 10UF 20% 4V X6S 0402	NO STUFF C1068 10UF 20% 4V X6S 0402	NO STUFF C1069 10UF 20% 4V X6S 0402	NO STUFF C1098 10UF 20% 4V X6S 0402	NO STUFF C1099 10UF 20% 4V X6S 0402	NO STUFF C109A 10UF 20% 4V X6S 0402							
NO STUFF C109B 10UF 20% 4V X6S 0402	NO STUFF C109C 10UF 20% 4V X6S 0402	NO STUFF C109D 10UF 20% 4V X6S 0402	NO STUFF C109E 10UF 20% 4V X6S 0402	NO STUFF C109F 10UF 20% 4V X6S 0402	NO STUFF C108A 10UF 20% 4V X6S 0402	NO STUFF C108B 10UF 20% 4V X6S 0402	NO STUFF C108C 10UF 20% 4V X6S 0402	NO STUFF C108D 10UF 20% 4V X6S 0402	NO STUFF C108E 10UF 20% 4V X6S 0402	NO STUFF C108F 10UF 20% 4V X6S 0402	NO STUFF C107A 10UF 20% 4V X6S 0402	NO STUFF C107B 10UF 20% 4V X6S 0402									

CRITICAL
C1031
470UF-0.0045OHM
20%
2.5V
POLY-TANT
SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

40 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF	C1041 2.2UF 20% 6.3V CERM 402-LF	C1042 2.2UF 20% 6.3V CERM 402-LF	C1043 2.2UF 20% 6.3V CERM 402-LF

C1050 10UF 20% 6.3V CERM-X5R 0402-1	C1051 10UF 20% 6.3V CERM-X5R 0402-1	C1052 10UF 20% 6.3V CERM-X5R 0402-1	C1053 10UF 20% 6.3V CERM-X5R 0402-1	C1054 10UF 20% 6.3V CERM-X5R 0402-1	C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM

NO STUFF
C1061 270UF 20% 2V TANT CASE-B2-SM

2x Bulk nostuff per Harris Beach v1.0 schematic

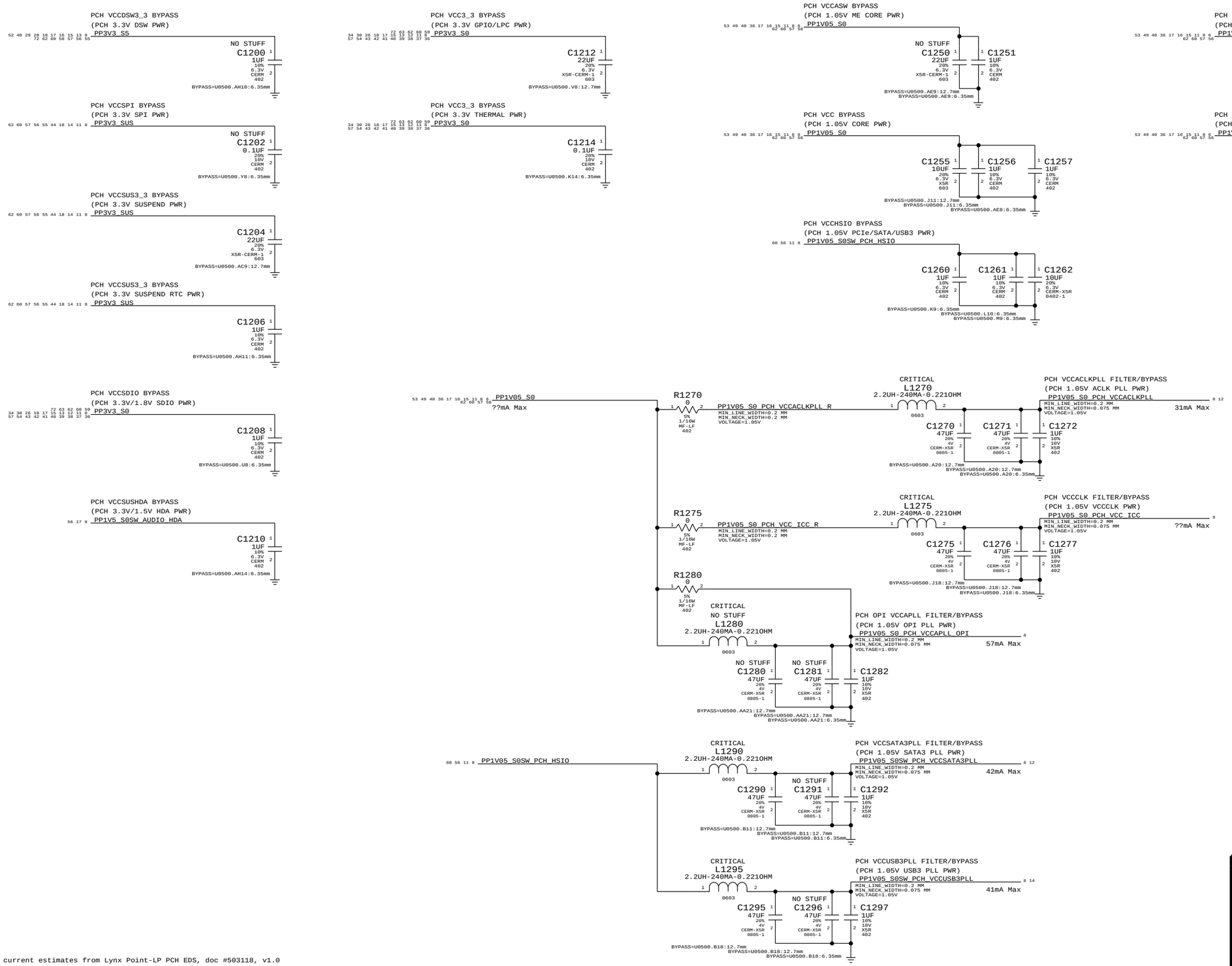
SYNC_MASTER=LABEL_J41 SYNC_DATE=01/11/2013

PAGE TITLE
CPU Decoupling

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 10 OF 120
SHEET 10 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

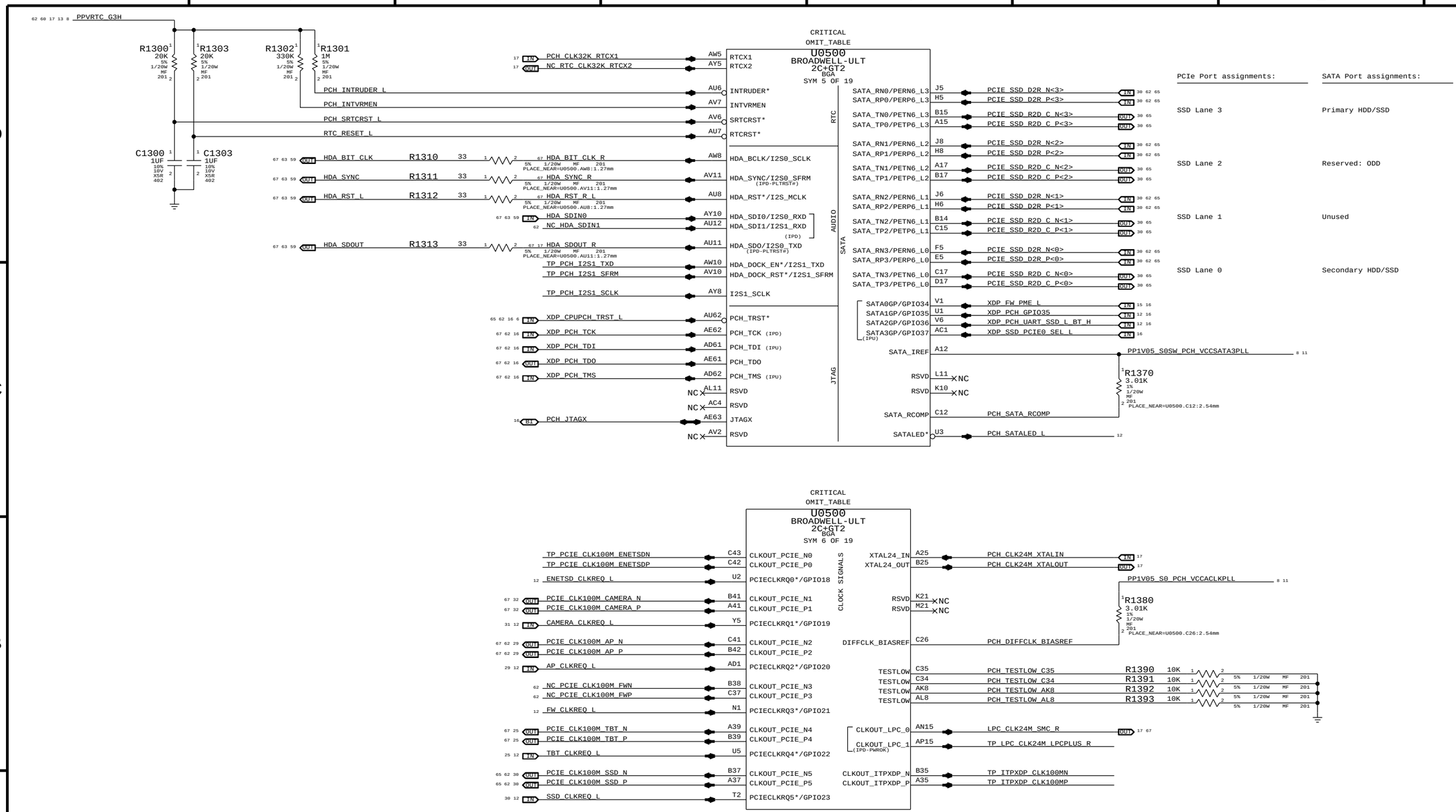
SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

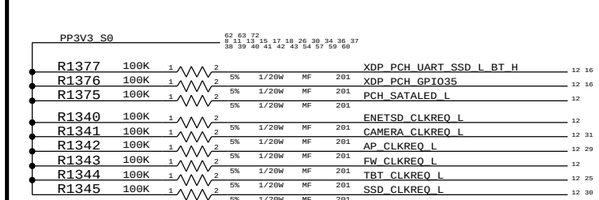
PAGE TITLE
PCH Decoupling

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 12 OF 120
SHEET 11 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





SYNC MASTER=WILL_J43 SYNC DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

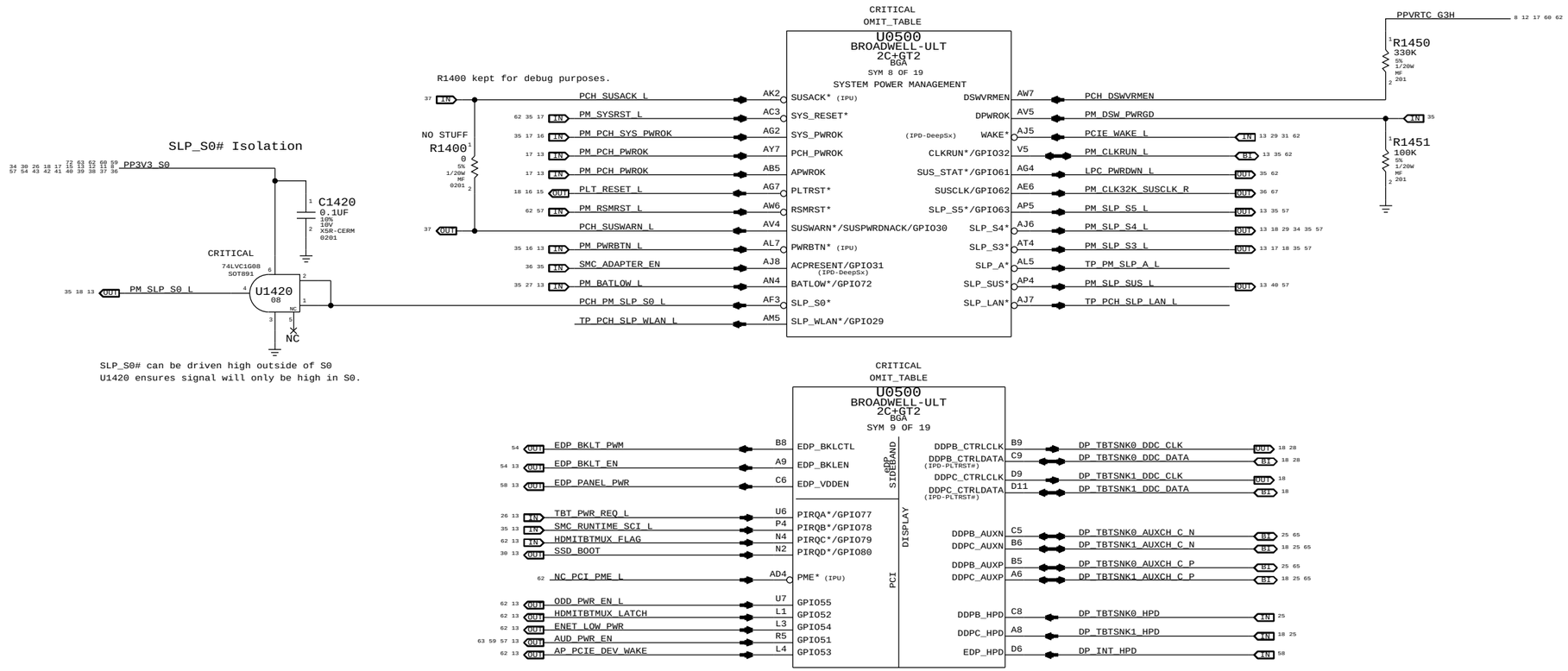
REVISION <E4LABEL>

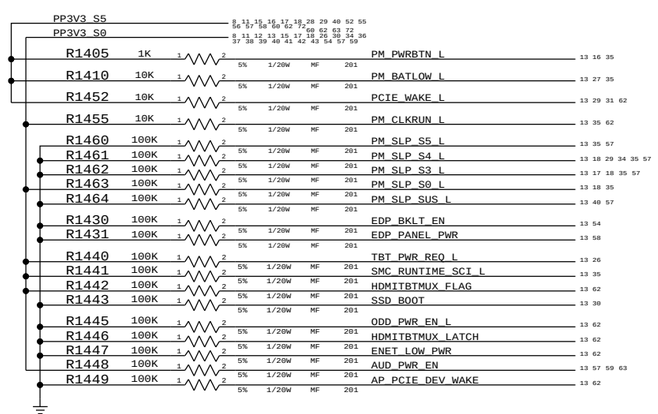
BRANCH <BRANCH>

PAGE 13 OF 120

SHEET 12 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





SYNC MASTER=J43_MLB SYNC DATE=02/20/2013

PAGE TITLE

PCH PM/PCI/GFX

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

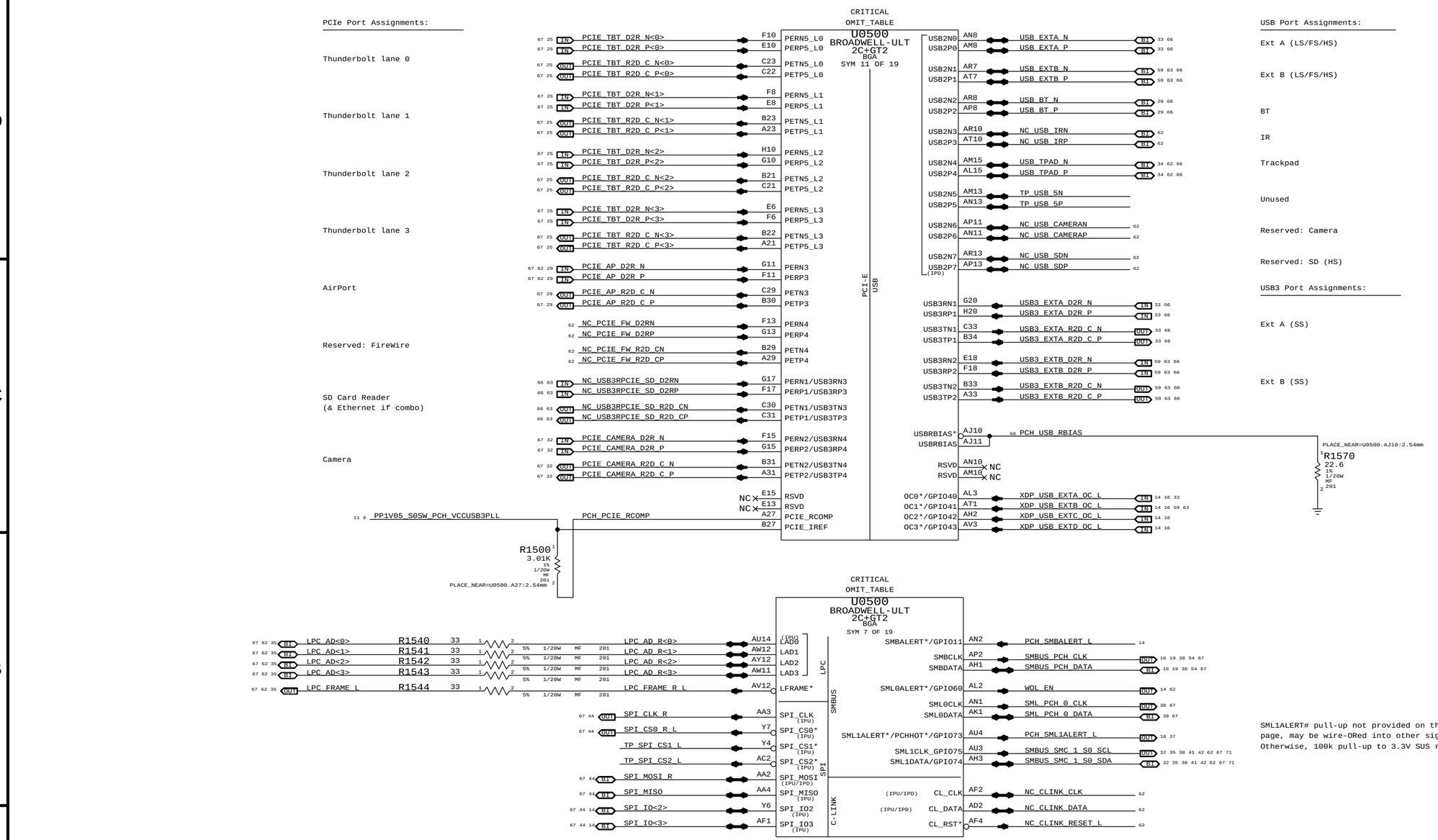
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 14 OF 120

SHEET 13 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=WILL_J43 SYNC DATE=09/13/2013

PAGE TITLE

PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

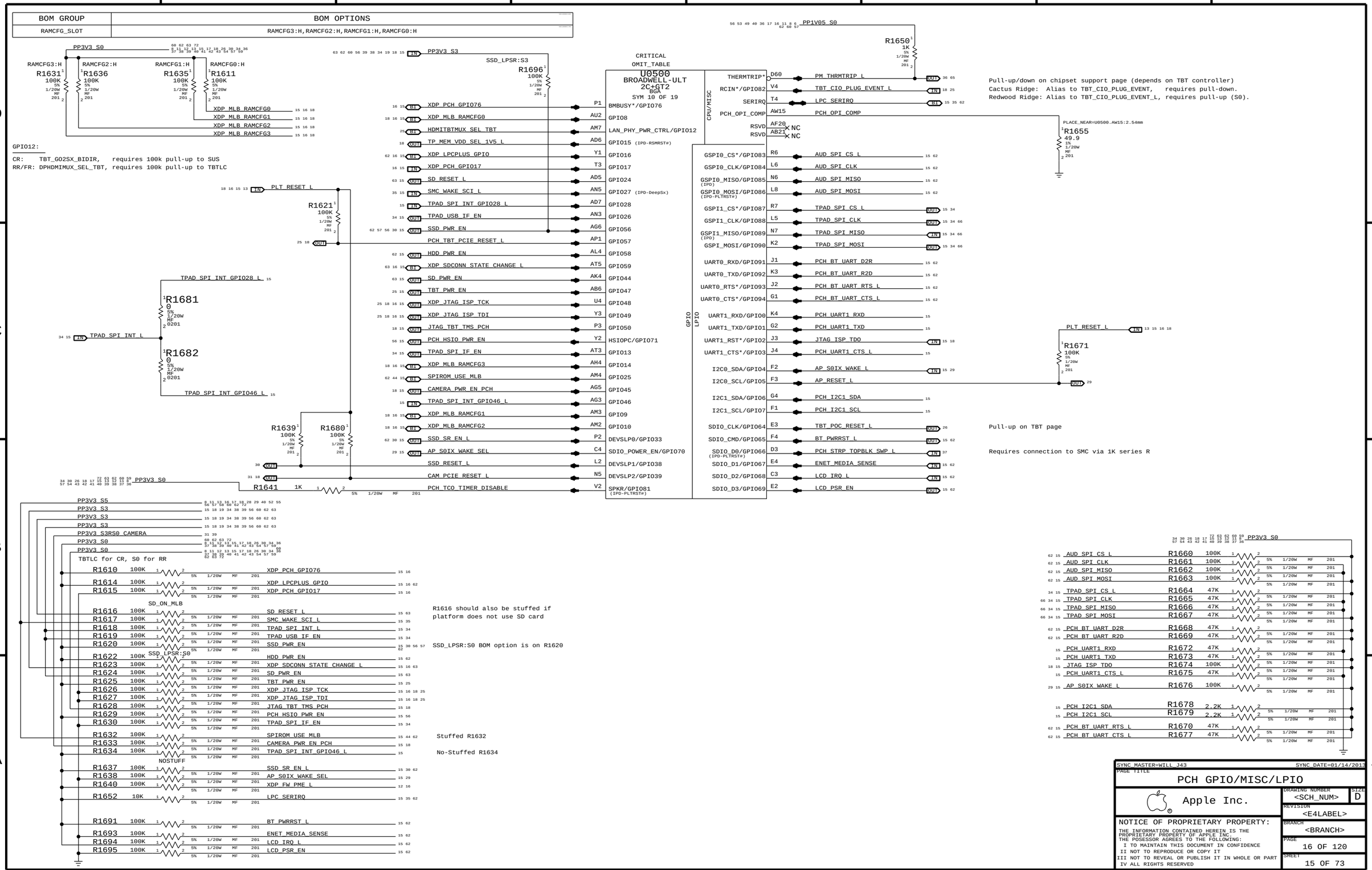
BRANCH <BRANCH>

PAGE 15 OF 120

SHEET 14 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H



SYNC MASTER=WILL J43 SYNC DATE=01/14/2013

PAGE TITLE

PCH GPIO/MISC/LPIO

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 16 OF 120

SHEET 15 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Extra BPM Testpoints

XDP_BPM_L<2>	TP1802	
XDP_BPM_L<3>	TP1803	
XDP_BPM_L<4>	TP1804	
XDP_BPM_L<5>	TP1805	
XDP_BPM_L<6>	TP1806	
XDP_BPM_L<7>	TP1807	

Merged (CPU/PCH) Micro2-XDP

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_PRESENT_L

CPU_VCCST_PWRGD	R1800	1K	XDP
PM_PWRBTN_L	R1802	0	XDP
PM_PCH_SYS_PWROK	R1804	0	XDP
XDP_CPU_TCK			
PCH_JTAGX	R1835	0	XDP

PLACE_NEAR=U0500.C61:2.54mm
PLACE_NEAR=U0500.J3:2.54mm
PLACE_NEAR=U0500.AG7:2.54mm
PLACE_NEAR=J1800.58:28mm

R1830	150	5% 1/16W MF-LF 402	
R1831	1K	5% 1/16W MF-LF 402	
C1804	0.1UF	10% 6.3V CERM-X5R 0201	XDP
C1800	0.1UF	10% 6.3V CERM-X5R 0201	XDP
C1801	0.1UF	10% 6.3V CERM-X5R 0201	XDP
C1806	0.1UF	10% 6.3V CERM-X5R 0201	XDP

XDP_CPU_TDO	R1810	51	XDP
XDP_CPU_TCK	R1813	51	XDP

PLACE_NEAR=U0500.F62:28mm
PLACE_NEAR=U0500.E60:28mm

TDI and TMS are terminated in CPU.

R1805	1K	XDP	PLT_RESET_L

PLACE_NEAR=U0500.AG7:2.54mm

CRITICAL XDP Q1840 DMN5L06VK-7 SOT563	PLACE_NEAR=J1800.51:28MM	XDP_CPU_TDO
CRITICAL XDP Q1840 DMN5L06VK-7 SOT563	MAKE_BASE=TRUE	XDP_CPUPCH_TRST_L
CRITICAL XDP Q1842 DMN5L06VK-7 SOT563	PLACE_NEAR=J1800.55:28mm	XDP_CPU_TDI
CRITICAL XDP Q1842 DMN5L06VK-7 SOT563		XDP_CPU_TMS

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L	MAKE_BASE=TRUE	XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE	XDP_JTAG_ISP_TCK
XDP_FW_PME_L	TP1879	
XDP_PCH_GPIO35	TP1880	
XDP_PCH_UART_SSD_L_BT_H	TP1881	
XDP_SSD_PCIE0_SEL_L	R1884 1K 5% 1/20W MF 201	
XDP_LPCPLUS_GPIO	MAKE_BASE=TRUE	XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE	XDP_JTAG_ISP_TDI

NOTE: Must not short XDP pins together!

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0	C1845	0.1UF 10% 16V X5R-CERM 0201
PP3V3_S5	R1845	330K 5% 1/20W MF 201
ALL_SYS_PWRGD	VCC U1845 74LVC1G07GF SOT891	XDP_JTAG_CPU_ISOL_L

NC NC NC NC

PP1V05_SUS			
PCH_JTAGX	R1899	1K	NO STUFF
XDP_PCH_TDO	R1890	51	XDP
XDP_PCH_TDI	R1891	51	XDP
XDP_PCH_TMS	R1892	51	XDP
XDP_PCH_TCK	R1896	51	NO STUFF
XDP_CPUPCH_TRST_L	R1897	51	NO STUFF

PLACE_NEAR=U0500.AE63:28mm
PLACE_NEAR=U0500.AE61:28mm
PLACE_NEAR=U0500.AD61:28mm
PLACE_NEAR=U0500.AD62:28mm
PLACE_NEAR=U0500.AE62:28mm
PLACE_NEAR=U0500.AU62:28mm

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE
CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 18 OF 120
SHEET 16 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support
new and old parts. With GreenCLK Rev C
pin 5 must receive S5 power (Stuff R2042)

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenCLK 25MHz Power
Must be powered if any VDDIO is powered.
PP3V3_S5RS3RS0_SYSCLKGEN

CAM XTAL Power
PP1V2_CAM_XTALPCIEVDD

TBT XTAL Power
PP3V3_TBTLC

C1924 0.1UF 10% 16V X5R-CERM 0201
C1922 0.1UF 10% 16V X5R-CERM 0201
C1902 1UF 20% 6.3V X5R 0201

CKPLUS_WAIVE=PwrTerm2Gnd

U1900
SLG3NB148CV
TQFN
CRITICAL

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

NC, VDD, VG3HOT
VIOE_25M_A, VIOE_25M_B, VIOE_25M_C
32.768K
25M_A, 25M_B, 25M_C
X2, X1
VOUT
GND, THRM PAD

PCH_CLK32K_RTCX1
SYSCLK_CLK25M_CAMERA
SYSCLK_CLK25M_TBT
PPVRTC_G3H
For SB RTC Power

C1910 1UF 20% 6.3V X5R 0201

NC_RTC_CLK32K_RTCX2
MAKE_BASE=TRUE
NO_TEST=TRUE

C1905 12PF 5% 25V NP0-C0G-CERM 0201
C1906 12PF 5% 25V NP0-C0G-CERM 0201

SYSCLK_CLK25M_X2
SYSCLK_CLK25M_X2_R
SYSCLK_CLK25M_X1

R1905 0 5% 1/20W MF 0201
NO STUFF
R1906 1M 5% 1/20W MF 201

CRITICAL
Y1905
25.000MHZ-12PF-20PPM
SM-3.2X2.5MM

NOTE: 30 PPM or better required for RTC accuracy

PCH 24MHz Crystal

C1915 6.8PF +/-0.1PF 25V C0G 0201
C1916 6.8PF +/-0.1PF 25V C0G 0201

PCH_CLK24M_XTALOUT_R
R1915 0 5% 1/20W MF 0201
PCH_CLK24M_XTALOUT

CRITICAL
Y1915
24.000MHZ-20PPM-6PF
3.20X2.50MM-SM1

R1916 1M 5% 1/20W MF 201
PCH_CLK24M_XTALIN

PCH 24MHz Outputs

LPC_CLK24M_SMC_R
PLACE_NEAR=U0500.AN15:5.1mm
R1927 22 5% 1/20W MF 201
LPC_CLK24M_SMC
MAKE_BASE=TRUE

PCH Reset Button

PP3V3_S0
R1995 10K 5% 1/20W MF 201
XDP
R1996 0 1/20W 0201 MF 5%
XDP_DBRESET_L
PM_SYSRST_L
NO STUFF
R1997 0 5% 1/16W MF-LF 402
SILK_PART=SYS RESET

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

PP1V2_S3
C1970 0.1UF 10% 16V X5R-CERM 0201
U1970 74AUP1G07GF SOT891
CPU_MEMVTT_PWR_EN_LSVDDQ

PP3V3_S0
R1970 330K 5% 1/20W MF 201

TPS51916 I(leak) = +/- 1uA,
Vih(min) = 1.8V
33uW when driven-low

MEMVTT_PWR_EN
MAKE_BASE=TRUE
MEMVTT_PWR_EN

PCH ME Disable Strap

PP5V_S0
R1920 100K 5% 1/20W MF 201

Q1920 DMN5L06VK-7 SOT563 VER 3
SPI_DESCRIPTOR_OVERRIDE_LS5V
PP1V5_S0SW_AUDIO_HDA
SPI_DESCRIPTOR_OVERRIDE

Q1920 DMN5L06VK-7 SOT563 VER 3

R1921 1K 5% 1/20W MF 201
HDA_SDOUT_R
IPD = 9-50k

SPI_DESCRIPTOR_OVERRIDE_L

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD

PP3V3_S5
C1930 0.1UF 10% 16V X5R-CERM 0201
CRITICAL
U1930 74AUP1G09 SOT891
ALL_SYS_PWRGD
PM_SLP_S3_L

PP1V05_S0
R1931 10K 5% 1/20W MF 201
CPU_VCCST_PWRGD

PCH PWROK Generation

PP3V42_G3H
PP3V3_S0
CPU_VR_EN
R1955 10K 5% 1/20W MF 201
NO STUFF
R1951 0 5% 1/20W MF 0201
CPU_VR_READY
MAKE_BASE=TRUE
CPU_VR_READY

R1950 10K 5% 1/20W MF 201
ALL_SYS_PWRGD
CPUVR_PGOOD_R

C1950 0.1UF 10% 16V X5R-CERM 0201
BYPASS=U1950:5MM
U1950 74LVC2G08GT SOT833
PM_S0_PGOOD

R1963 0 5% 1/20W MF 0201
NO STUFF
R1961 100K 5% 1/20W MF 201

NO STUFF
R1960 0 5% 1/20W MF 0201
WF: Do we need this?
CKPLUS_WAIVE=UNCONNECTED_PINS
U1950 74LVC2G08GT SOT833
SYS_PWROK_R
CKPLUS_WAIVE=UNCONNECTED_PINS

R1962 1K 5% 1/20W MF 201
PM_PCH_SYS_PWROK

PM_PCH_PWROK
MAKE_BASE=TRUE

SMC_DELAYED_PWRGD

SYNC_MASTER=J43_MLB1	SYNC_DATE=01/09/2013
PAGE TITLE: Chipset Support	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH: <BRANCH>
	PAGE: 19 OF 120
	SHEET: 17 OF 73

Platform Reset Connections

Unbuffered

PLT_RESET_L → R2071 0 5% 1/20W MF 0201 → PCA9557D_RESET_L

Scrub for Layout Optimization

Buffered

PP3V3_S0 → C2071 0.1UF 10% 16V X5R-CERM 0201; U2071 CRITICAL MC74VHC1G08 SC70-HF; R2070 100K 5% 1/20W MF 201

PLT_RST_BUF_L → R2072 0 5% 1/20W MF 0201 → SMC_LRESET_L

R2088 0 5% 1/20W MF 0201 → BKLT_PLT_RST_L

NOSTUFF R2089 0 5% 1/20W MF 0201 → CAM_PCIE_RESET_L

PCH_TBT_PCIE_RESET_L (MAKE_BASE=TRUE) → PCH_TBT_PCIE_RESET_L

PP3V3_S5 → NOSTUFF C2030 0.1UF 10% 10V X5R-CERM 0201 (BYPASS=U2030:3mm)

PM_SLP_S4_L, CAMERA_PWR_EN_PCH → NOSTUFF CRITICAL U2030 74LVC1G08 SOT891 → CAMERA_PWR_EN; NC

R2030 0 5% 1/20W MF 0201

Power State Debug LEDs

(For development only)

PP3V3_S5 → DBGLED R2094 0 5% 1/16W MF-LF 402 (PLACE_SIDE=BOTTOM) → PP3V3_S5_DBGLED (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED R2090 20K	DBGLED R2091 20K	DBGLED R2092 20K	DBGLED R2093 20K	DBGLED R2095 20K	5% 1/20W MF 201
DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0I3	DBGLED_S0	
DBGLED D2090 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S5_ON	DBGLED D2091 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=STBY_ON	DBGLED D2092 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S3_ON	DBGLED D2093 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0I3_ON	DBGLED D2095 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0_ON	
	DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0I3_D	DBGLED_S0_D	
	DBGLED Q2090 DMN5L06VK-7 SOT563 VER 3	DBGLED Q2090 DMN5L06VK-7 SOT563 VER 3	DBGLED Q2091 DMN5L06VK-7 SOT563 VER 3	DBGLED Q2091 DMN5L06VK-7 SOT563 VER 3	

S4_PWR_EN, PM_SLP_S4_L, PM_SLP_S3_L, PM_SLP_S0_L

GreenCLK 25MHz Power

PP3V3_S3 → NO STUFF R2040 0 5% 1/20W MF 0201 → PP3V3_S5RS3RS0_SYSCLKGEN

PP3V3_S5RS3RS0_SYSCLKGEN (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)

PP3V3_S0 → NO STUFF R2041 0 5% 1/20W MF 0201

PP3V3_S5 → R2042 0 5% 1/20W MF 0201

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

PP3V3_TBTLC → R2061 100K 5% 1/20W MF 201; C2060 0.1UF 20% 10V CERM 402; R2062 100K 5% 1/20W MF 201

U2060 74LVC2G07 SOT891 (VCC, GND)

From RR: JTAG_TBT_TDO → JTAG_ISP_TDO → To PCH

From PCH: JTAG_TBT_TMS_PCH → JTAG_TBT_TMS → To RR

S0 pull-up on PCH page

NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary.

Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property

TP_CPU_RSVDN61 — TP_CPU_RSVDN61 (MAKE_BASE=TRUE)

TP_CPU_RSVDP61 — TP_CPU_RSVDP61 (MAKE_BASE=TRUE)

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0, XDP_MLB_RAMCFG1, XDP_MLB_RAMCFG2, XDP_MLB_RAMCFG3

RAMCFG3:L	RAMCFG2:L	RAMCFG1:L	RAMCFG0:L
R2050 10K	R2051 10K	R2052 10K	R2053 10K

5% 1/20W MF 201

LPDDR3 Alias Support

TP_CPU_MEM_RESET_L	TP_CPU_MEM_RESET_L	MAKE_BASE=TRUE
TP_MEM_VDD_SEL_1V5_L	TP_MEM_VDD_SEL_1V5_L	MAKE_BASE=TRUE
PP0V6_S3_MEM_VREFDQ_A	PP0V6_S3_MEM_VREFDQ_A	MAKE_BASE=TRUE, VOLTAGE=0.6V
PP0V6_S3_MEM_VREFCA_A	PP0V6_S3_MEM_VREFCA_A	MAKE_BASE=TRUE, VOLTAGE=0.6V
PP0V6_S3_MEM_VREFDQ_B	PP0V6_S3_MEM_VREFDQ_B	MAKE_BASE=TRUE, VOLTAGE=0.6V
PP0V6_S3_MEM_VREFCA_B	PP0V6_S3_MEM_VREFCA_B	MAKE_BASE=TRUE, VOLTAGE=0.6V

DDC Pull-Ups

2.2k pull-ups are required by PCH to indicate active display interface.

DP++ spec violation, should remove!

PP3V3_S0 → NO STUFF R2020 2.2K; R2021 2.2K; NO STUFF R2022 2.2K; R2023 2.2K (5% 1/20W MF 201)

DP_TBTSNK0_DDC_CLK, DP_TBTSNK0_DDC_DATA, DP_TBTSNK1_DDC_CLK, DP_TBTSNK1_DDC_DATA

TBTSNK1_DDC is pulled-up just to indicate that DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so DDC_CLK pull-ups are unstuffed.

Thunderbolt Pull-up/downs

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC (on TBT page)

PP3V3_S0 → R2015 100K 5% 1/20W MF 201

Falcon Ridge PLUG_EVENT is active-low, always driven (pull-up)

TBT_CIO_PLUG_EVENT_L (MAKE_BASE TRUE) TBT_CIO_PLUG_EVENT_L

Required for unused second TBT port

TBT_B_CIO_SEL, DP_TBTPB_HPD, TBT_B_CONFIG2_RC, TBT_B_CONFIG1_BUF, TBT_B_LSRX

R2016 10K	R2017 10K	R2018 10K	R2019 10K	R2014 10K

5% 1/20W MF 201

TBT Aliases

DP_TBTSNK0_DDC_CLK	DP_TBTSNK0_DDC_CLK	MAKE_BASE TRUE
DP_TBTSNK0_DDC_DATA	DP_TBTSNK0_DDC_DATA	MAKE_BASE TRUE
DP_TBTSNK1_HPD	DP_TBTSNK1_HPD	MAKE_BASE TRUE
=DP_TBTSNK1_ML_C_P<3..0>	DP_TBTSNK1_ML_C_P<3..0>	TRUE
=DP_TBTSNK1_ML_C_N<3..0>	DP_TBTSNK1_ML_C_N<3..0>	TRUE
DP_TBTSNK1_AUXCH_C_P	DP_TBTSNK1_AUXCH_C_P	TRUE
DP_TBTSNK1_AUXCH_C_N	DP_TBTSNK1_AUXCH_C_N	TRUE
DP_TBTSNK1_DDC_CLK	DP_TBTSNK1_DDC_CLK	TRUE
DP_TBTSNK1_DDC_DATA	DP_TBTSNK1_DDC_DATA	TRUE

Single-port TBT implementation does not require DDC Crossbar

XDP_JTAG_ISP_TCK — XDP_JTAG_ISP_TCK

XDP_JTAG_ISP_TDI — XDP_JTAG_ISP_TDI

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

PP3V3_SUS → R2010 100K 5% 1/20W MF 201 → PCH_SML1ALERT_L

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: Project Chipset Support

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 20 OF 120
SHEET 18 OF 73

Page Notes

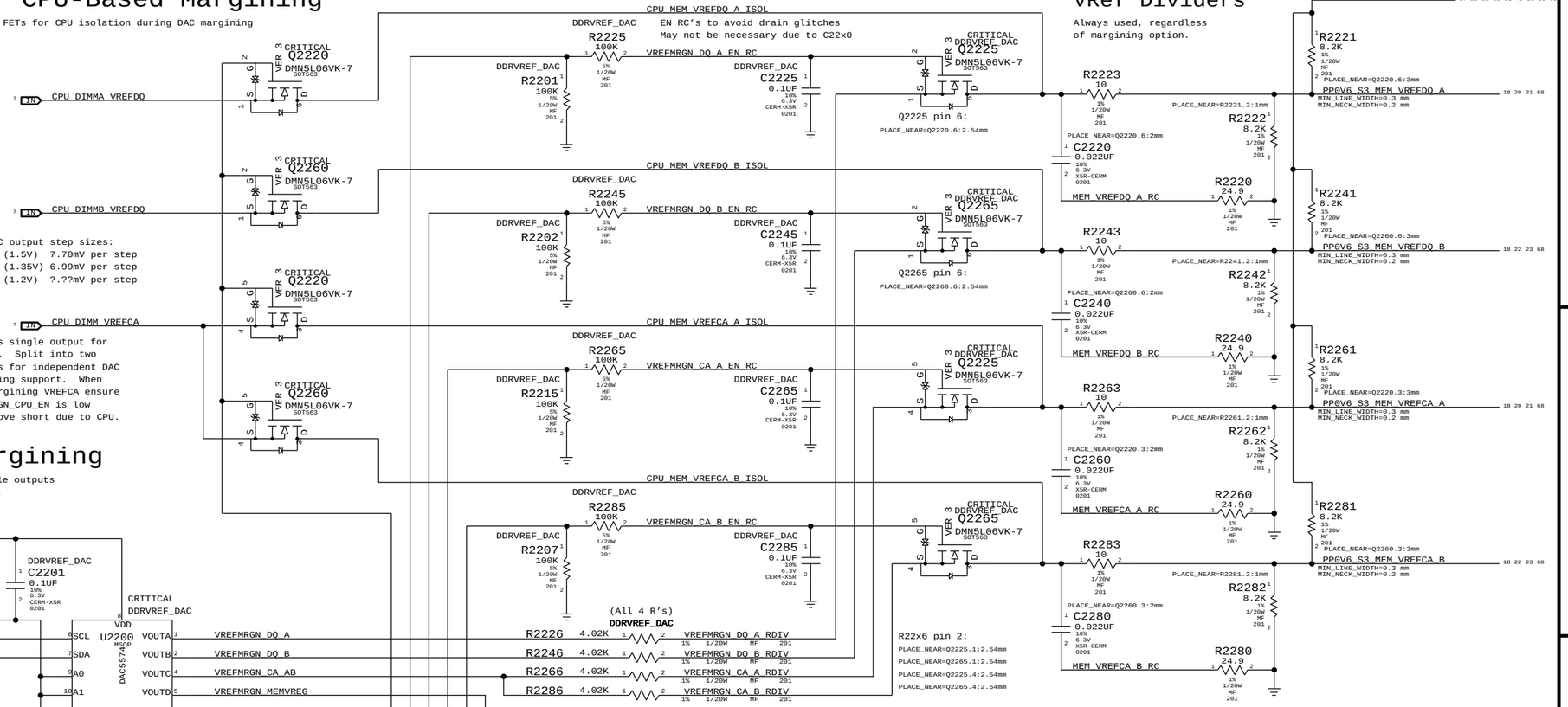
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining



NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

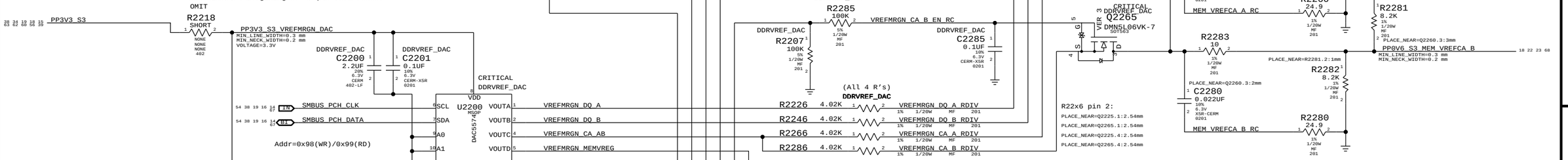
VRef Dividers

Always used, regardless of margining option.

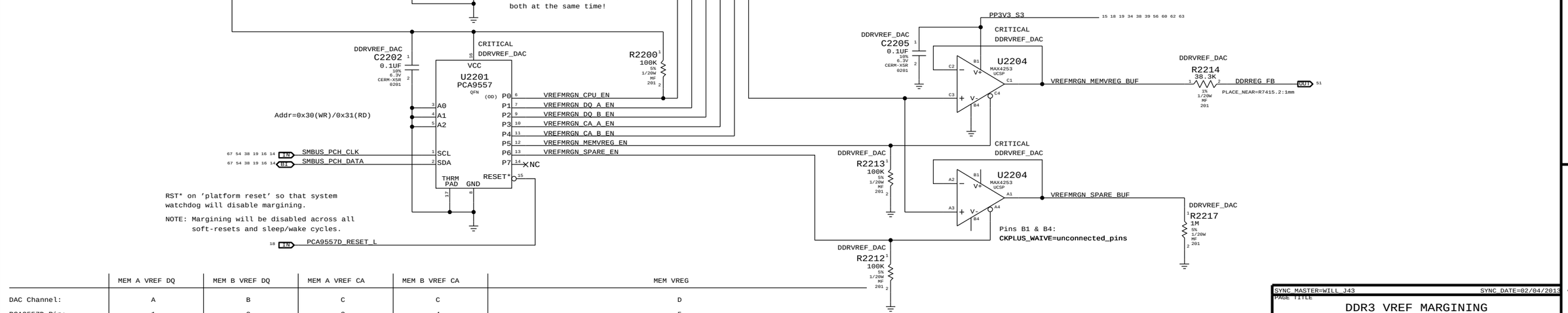
DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

OMIT



NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!



RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

SYNC_MASTER=WILL_J43 SYNC_DATE=02/04/2013

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

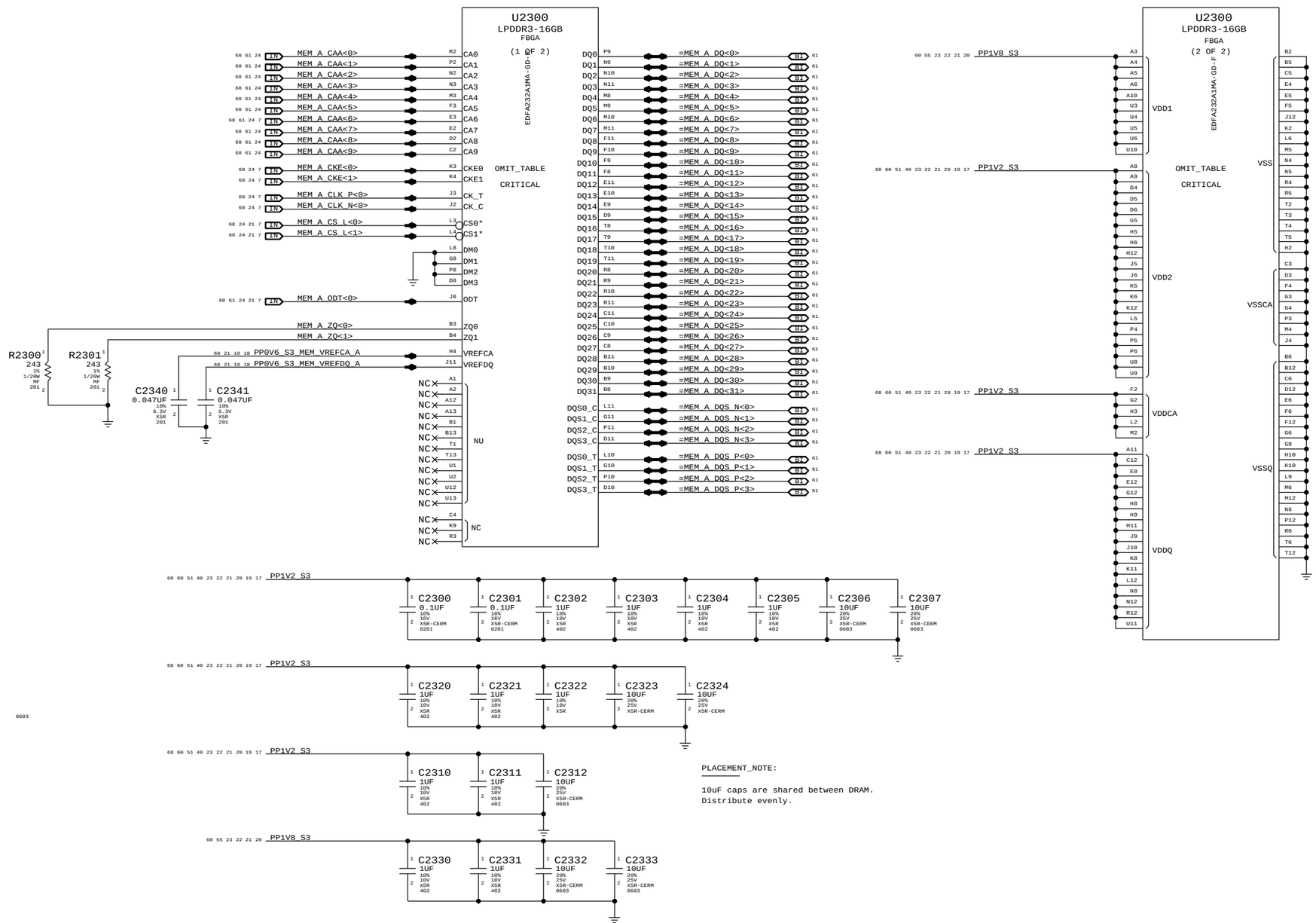
BRANCH: <BRANCH>

PAGE: 22 OF 120

SHEET: 19 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

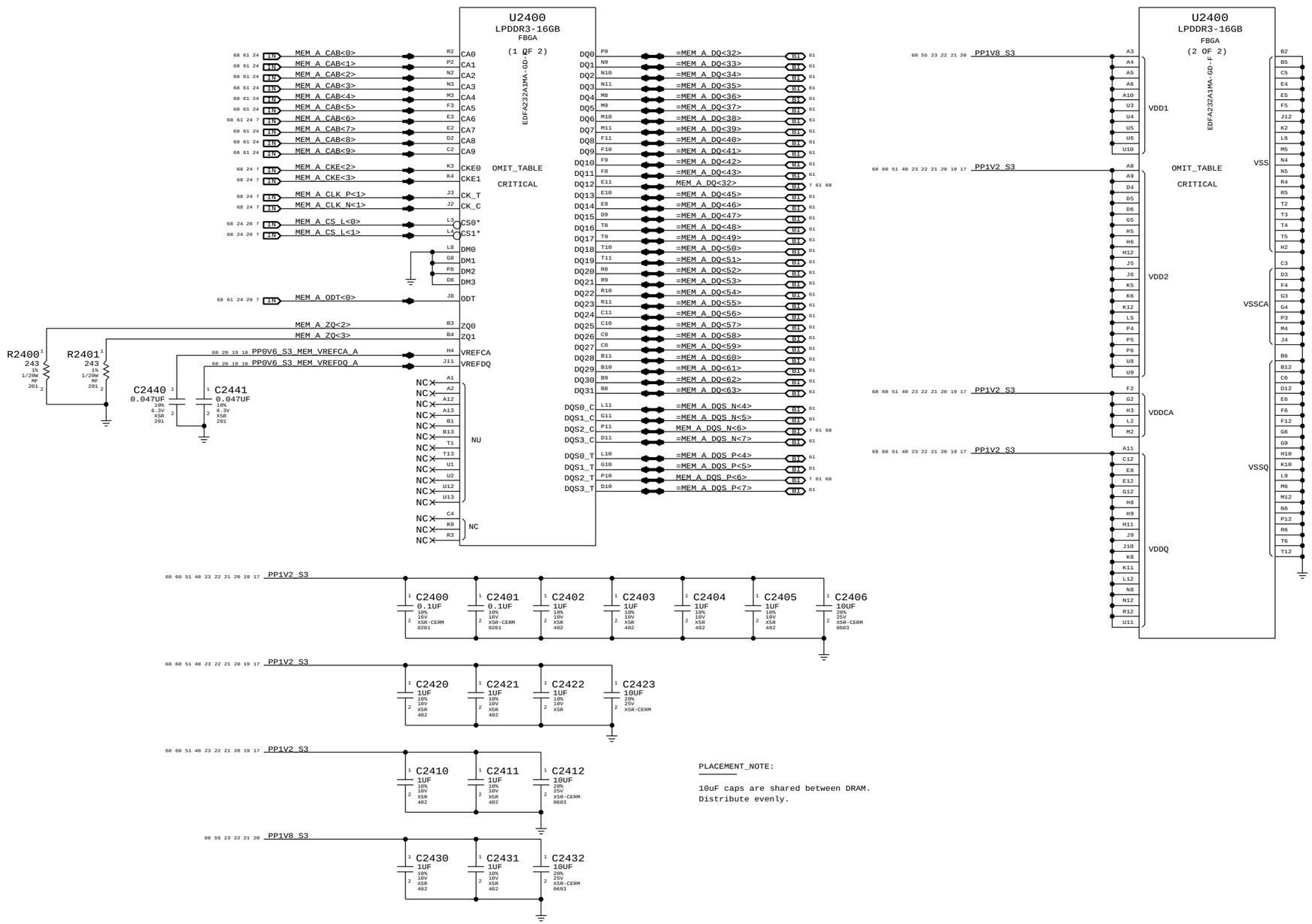
PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 23 OF 120
SHEET 20 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

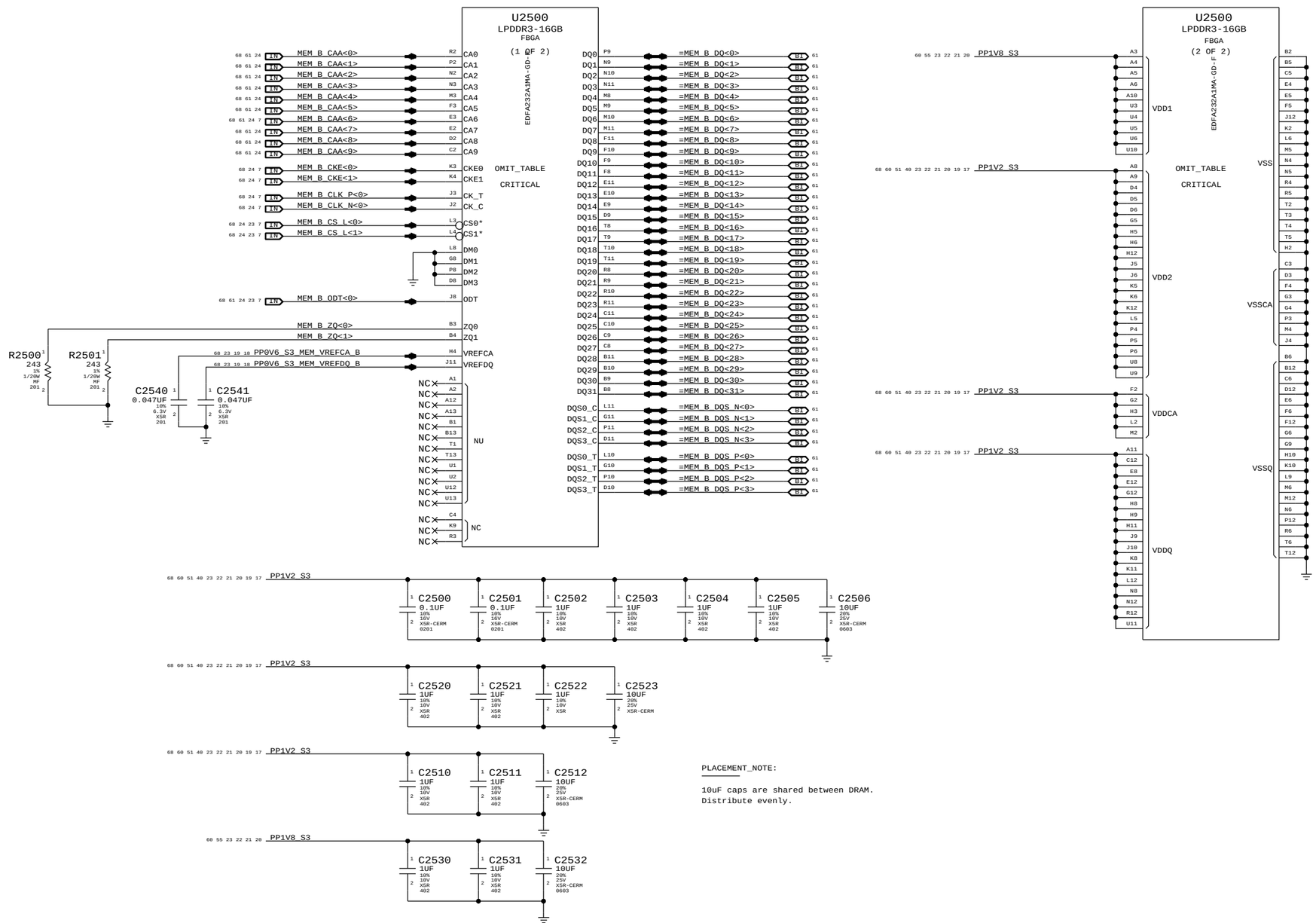
PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 24 OF 120
SHEET 21 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

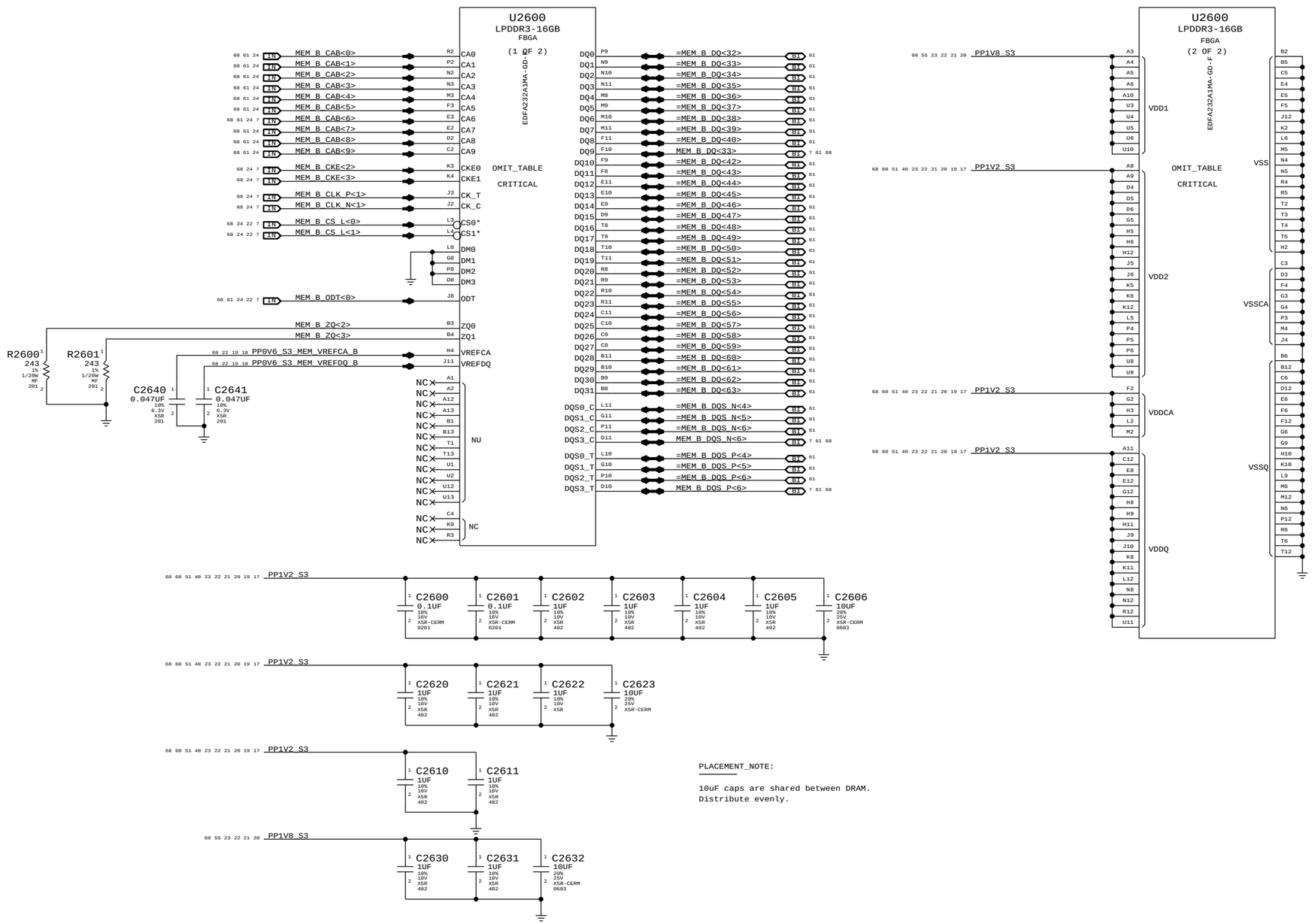
PAGE TITLE
LPDDR3 DRAM Channel B (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 25 OF 120
SHEET 22 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

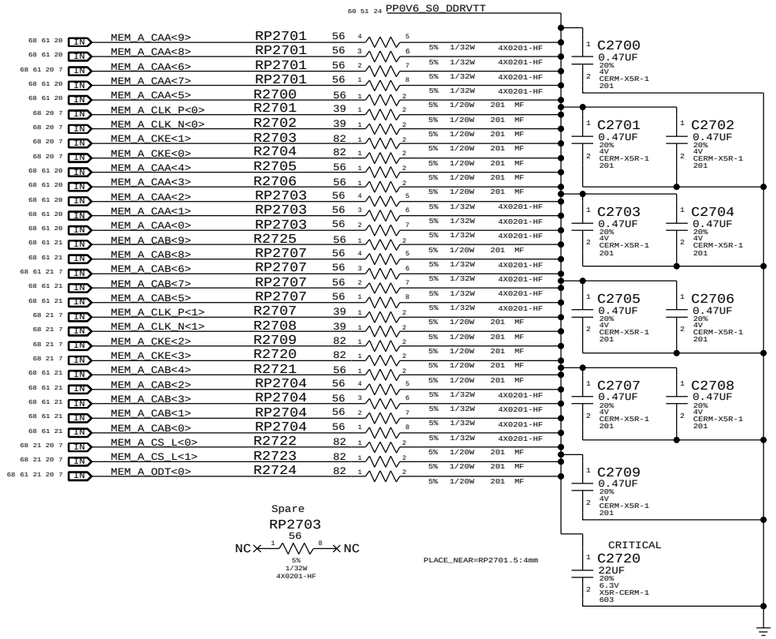
PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

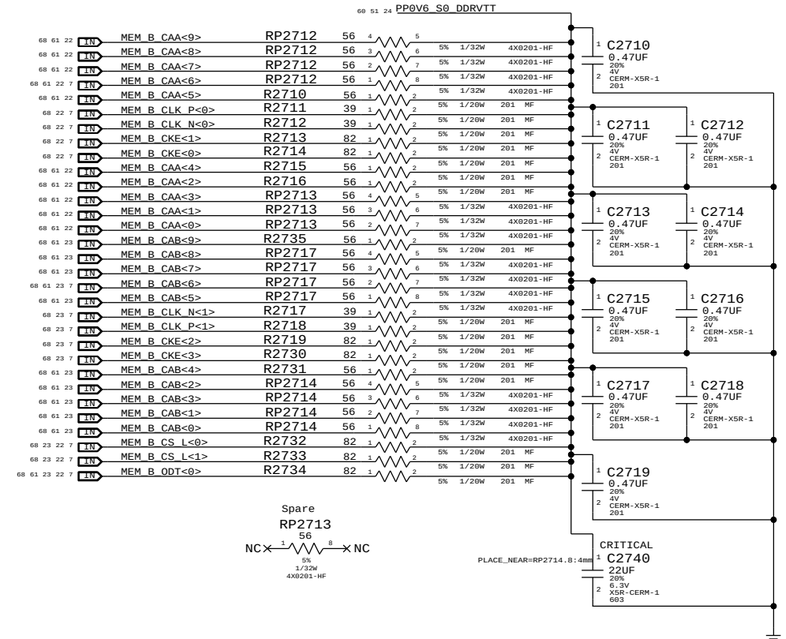
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 26 OF 120
SHEET 23 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC MASTER=J43_MLB SYNC DATE=09/21/2012

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

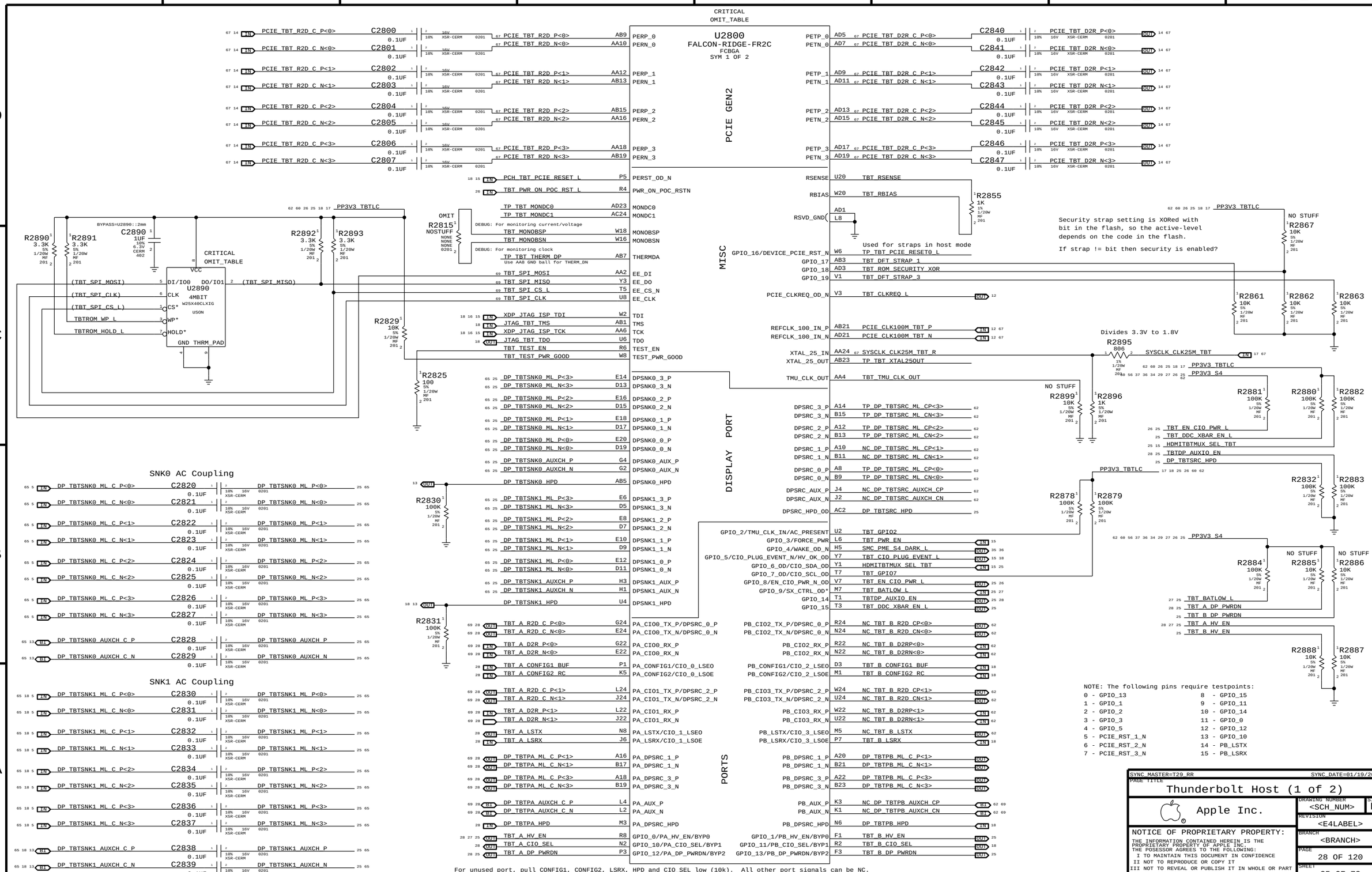
REVISION <E4LABEL>

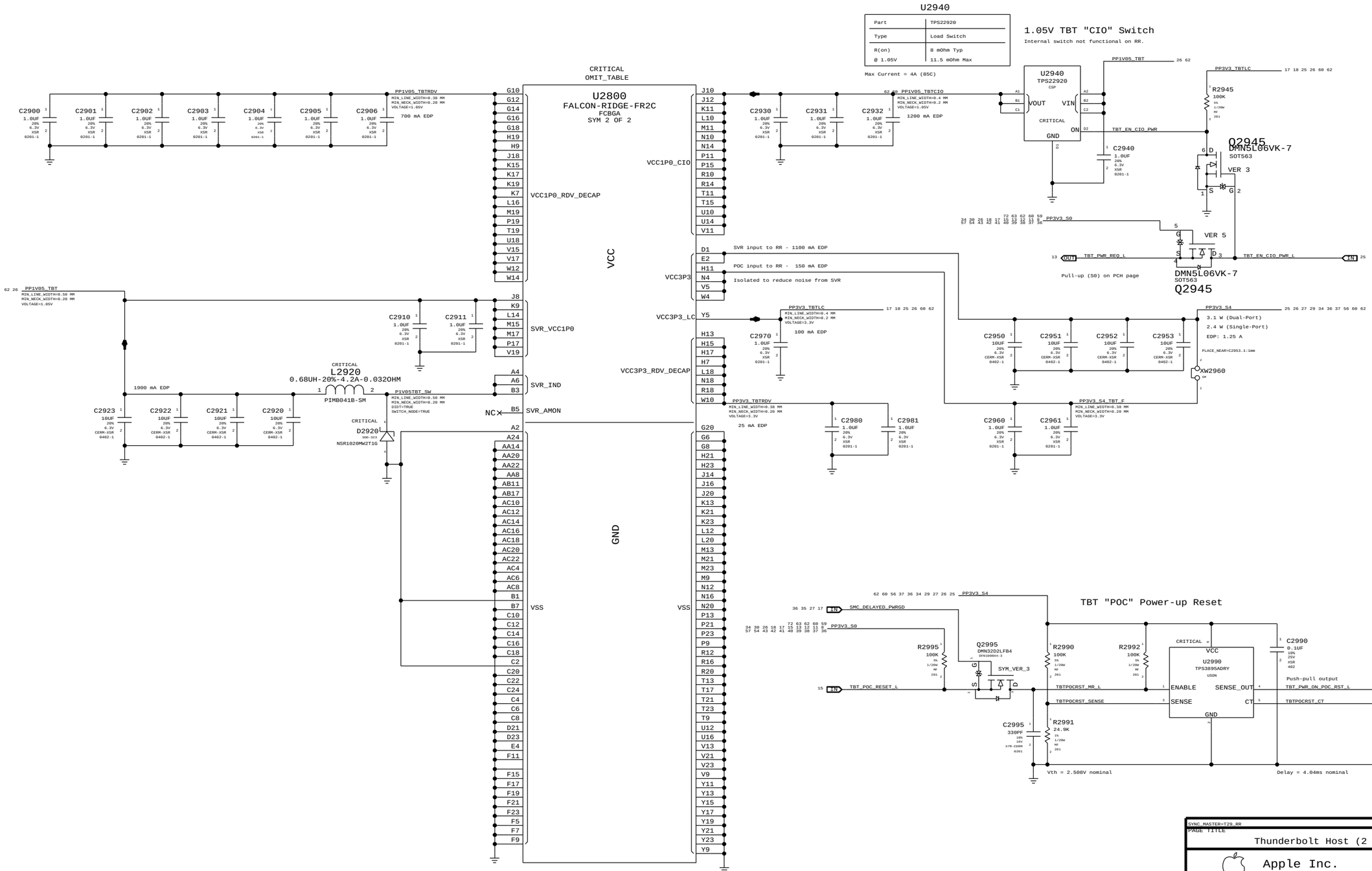
BRANCH <BRANCH>

PAGE 27 OF 120

SHEET 24 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


U2800
FALCON-RIDGE-FR2C
FCBGA
SYM 1 OF 2
CRITICAL
OMIT_TABLE
PCIE GEN2
MISC
DISPLAY PORT
PORTS
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_C_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_N<3>
PCH_TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TP_TBT_MONDC0
TP_TBT_MONDC1
DEBUG: For monitoring current/voltage
TBT_MONOBSP
TBT_MONOBSN
DEBUG: For monitoring clock
TP_TBT_THERM_DP
Use AA8 GND ball for THERM_DN
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
XDP_JTAG_ISP_TDI
JTAG_TBT_TMS
XDP_JTAG_ISP_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_HPD
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_HPD
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_CONFIG1_BUF
TBT_A_CONFIG2_RC
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_C_N
DP_TBTPA_HPD
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_RSENSE
TBT_RBIAS
R2855 1K
Used for straps in host mode
TP_TBT_PCIE_RESET0_L
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT_R
SYSCLK_CLK25M_TBT
TP_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
TP_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>
NC_DP_TBTSRC_ML_CP<1>
NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>
NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN
DP_TBTSRC_HPD
TBT_GPIO2
TBT_PWR_EN
SMC_PME_S4_DARK_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
TBT_BATLOW_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
NC_TBT_B_R2D_CP<0>
NC_TBT_B_R2D_CN<0>
NC_TBT_B_D2RP<0>
NC_TBT_B_D2RN<0>
TBT_B_CONFIG1_BUF
TBT_B_CONFIG2_RC
NC_TBT_B_R2D_CP<1>
NC_TBT_B_R2D_CN<1>
NC_TBT_B_D2RP<1>
NC_TBT_B_D2RN<1>
NC_TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
NC_DP_TBTPB_AUXCH_CP
NC_DP_TBTPB_AUXCH_CN
DP_TBTPB_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
PP3V3_TBTLC
BYPASS=U2890::2mm
R2890 3.3K
R2891 3.3K
C2890 1UF
R2892 3.3K
R2893 3.3K
OMIT
R2815 NOSTUFF
U2890 4MBIT W25X40CLXIG USON
(TBT_SPI_MOSI)
(TBT_SPI_MISO)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
R2829 10K
R2825 100
R2830 100K
R2831 100K
SNK0 AC Coupling
DP_TBTSNK0_ML_C_P<0>
DP_TBTSNK0_ML_C_N<0>
DP_TBTSNK0_ML_C_P<1>
DP_TBTSNK0_ML_C_N<1>
DP_TBTSNK0_ML_C_P<2>
DP_TBTSNK0_ML_C_N<2>
DP_TBTSNK0_ML_C_P<3>
DP_TBTSNK0_ML_C_N<3>
DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_AUXCH_C_N
SNK1 AC Coupling
DP_TBTSNK1_ML_C_P<0>
DP_TBTSNK1_ML_C_N<0>
DP_TBTSNK1_ML_C_P<1>
DP_TBTSNK1_ML_C_N<1>
DP_TBTSNK1_ML_C_P<2>
DP_TBTSNK1_ML_C_N<2>
DP_TBTSNK1_ML_C_P<3>
DP_TBTSNK1_ML_C_N<3>
DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
NO STUFF
R2867 10K
R2861 10K
R2862 10K
R2863 10K
Divides 3.3V to 1.8V
R2895 806
R2896 1K
R2899 10K
R2881 100K
R2880 100K
R2882 100K
R2878 100K
R2879 100K
R2832 100K
R2883 100K
R2884 100K
R2885 10K
R2886 10K
R2888 10K
R2887 10K
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
SYNC_MASTER=T29_RR
SYNC_DATE=01/19/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
28 OF 120
SHEET
25 OF 73
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=T29_RR SYNC_DATE=12/17/2012

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 29 OF 120

SHEET 26 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

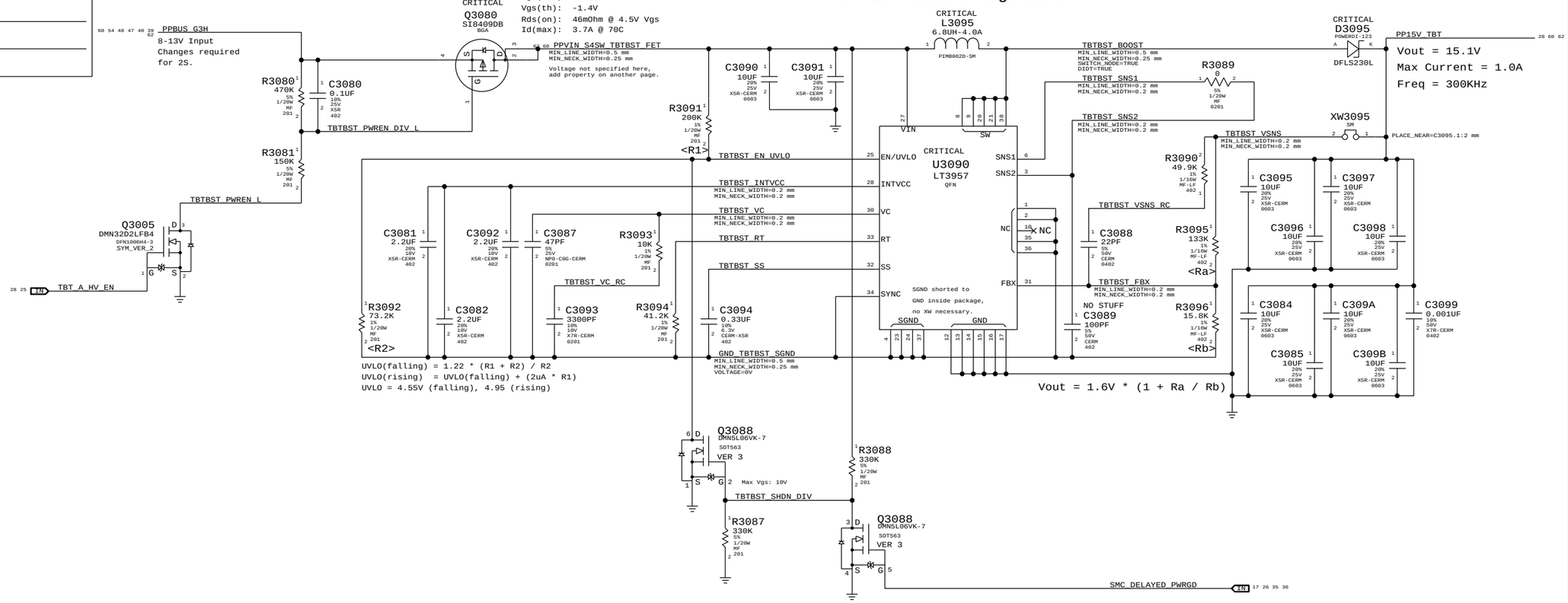
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

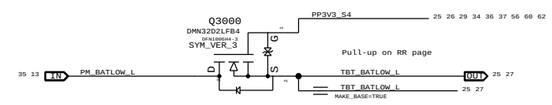
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

TBT 15V Boost Regulator



BATLOW# Isolation



SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: TBT Power Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 30 OF 120

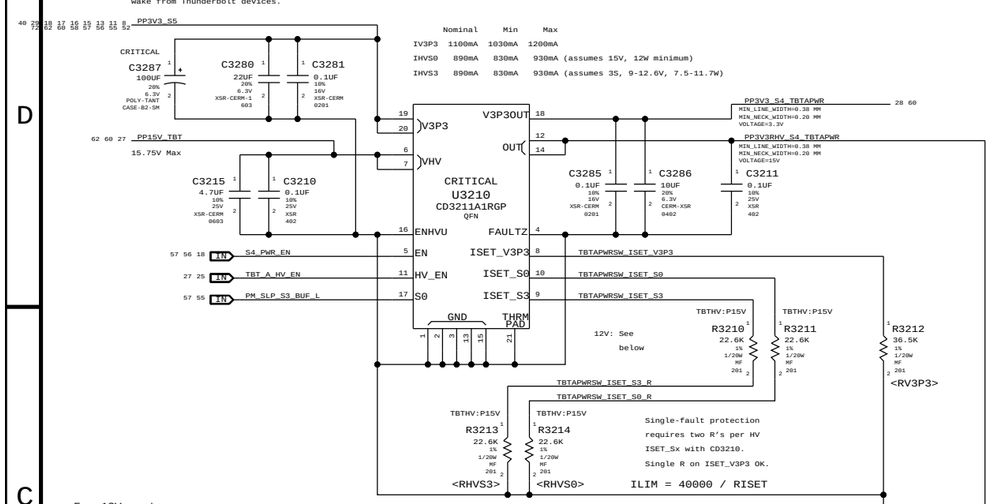
SHEET: 27 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

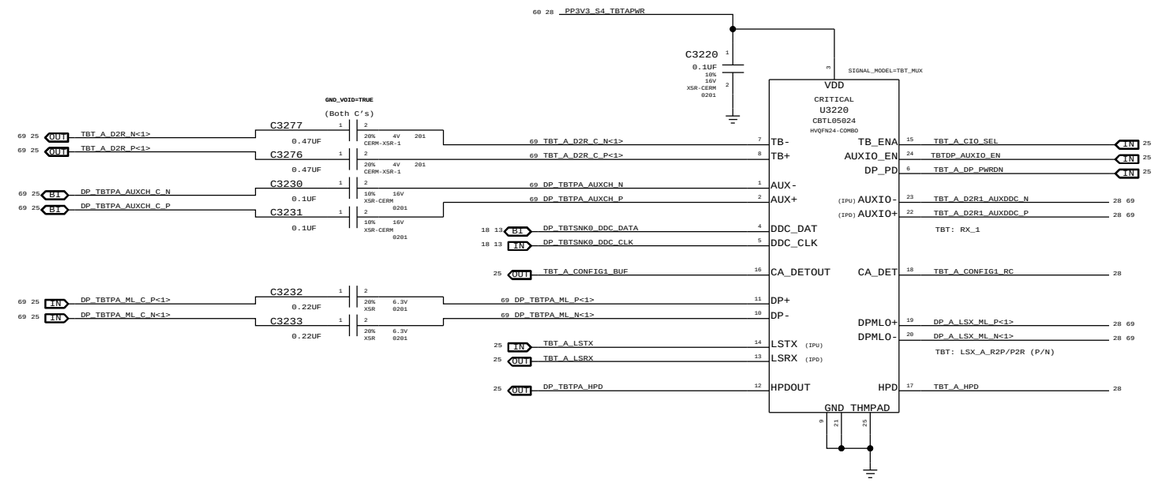
	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

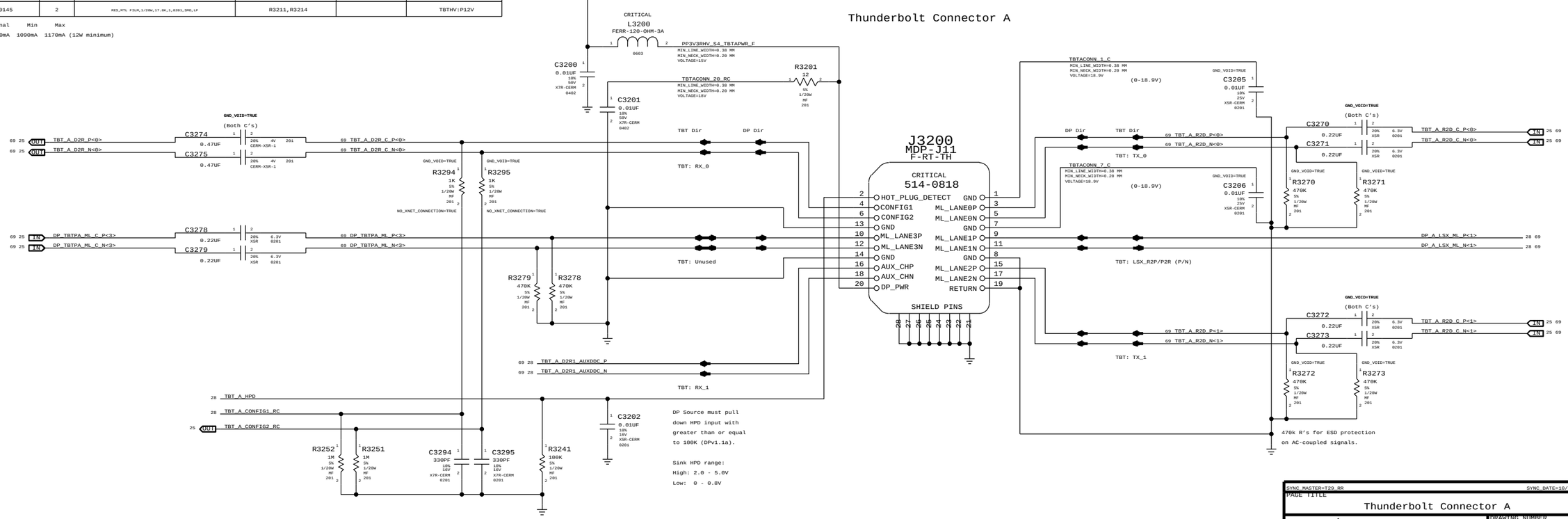


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)





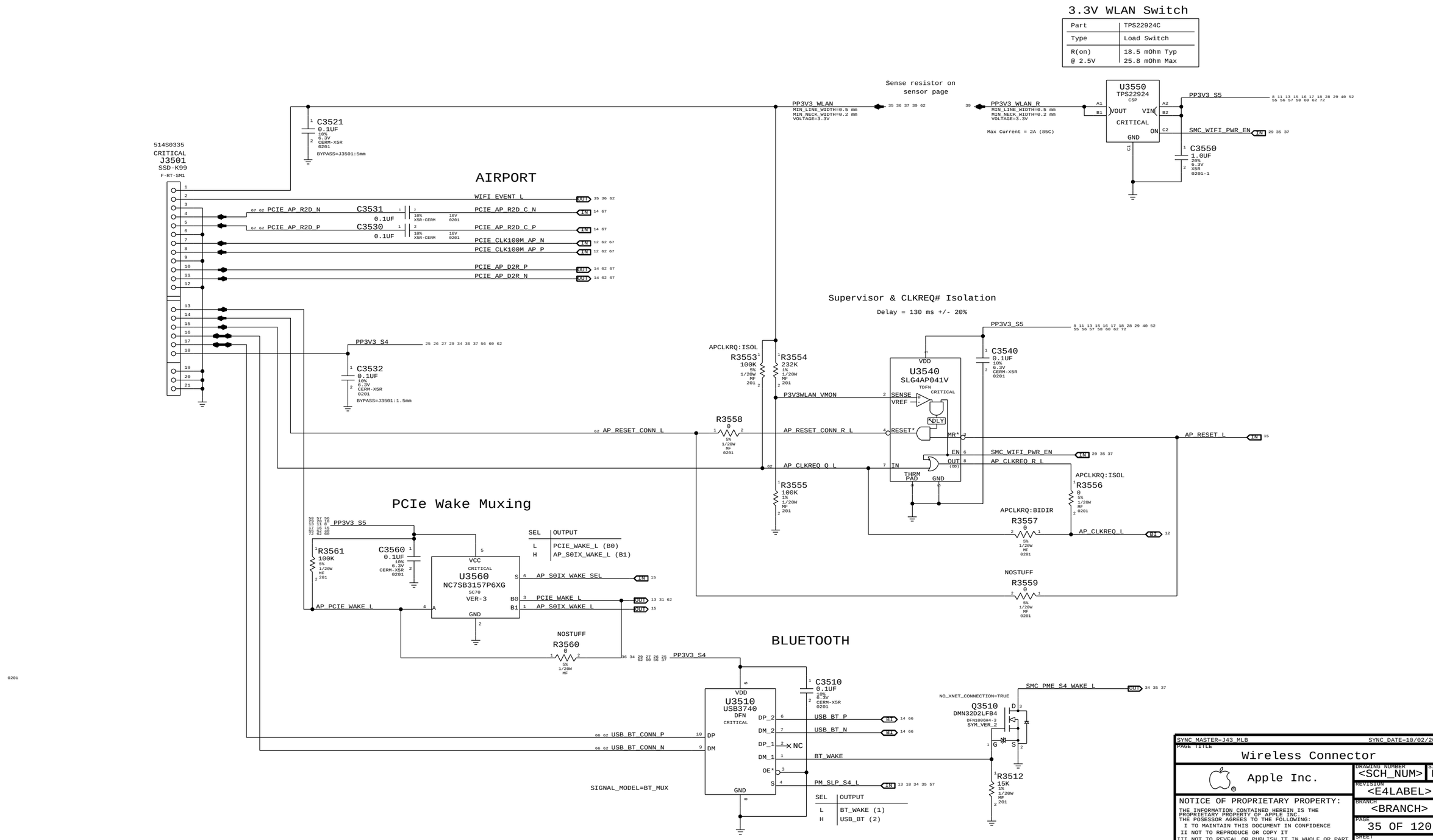
SYNC_MASTER=T29_RR SYNC_DATE=10/26/2012

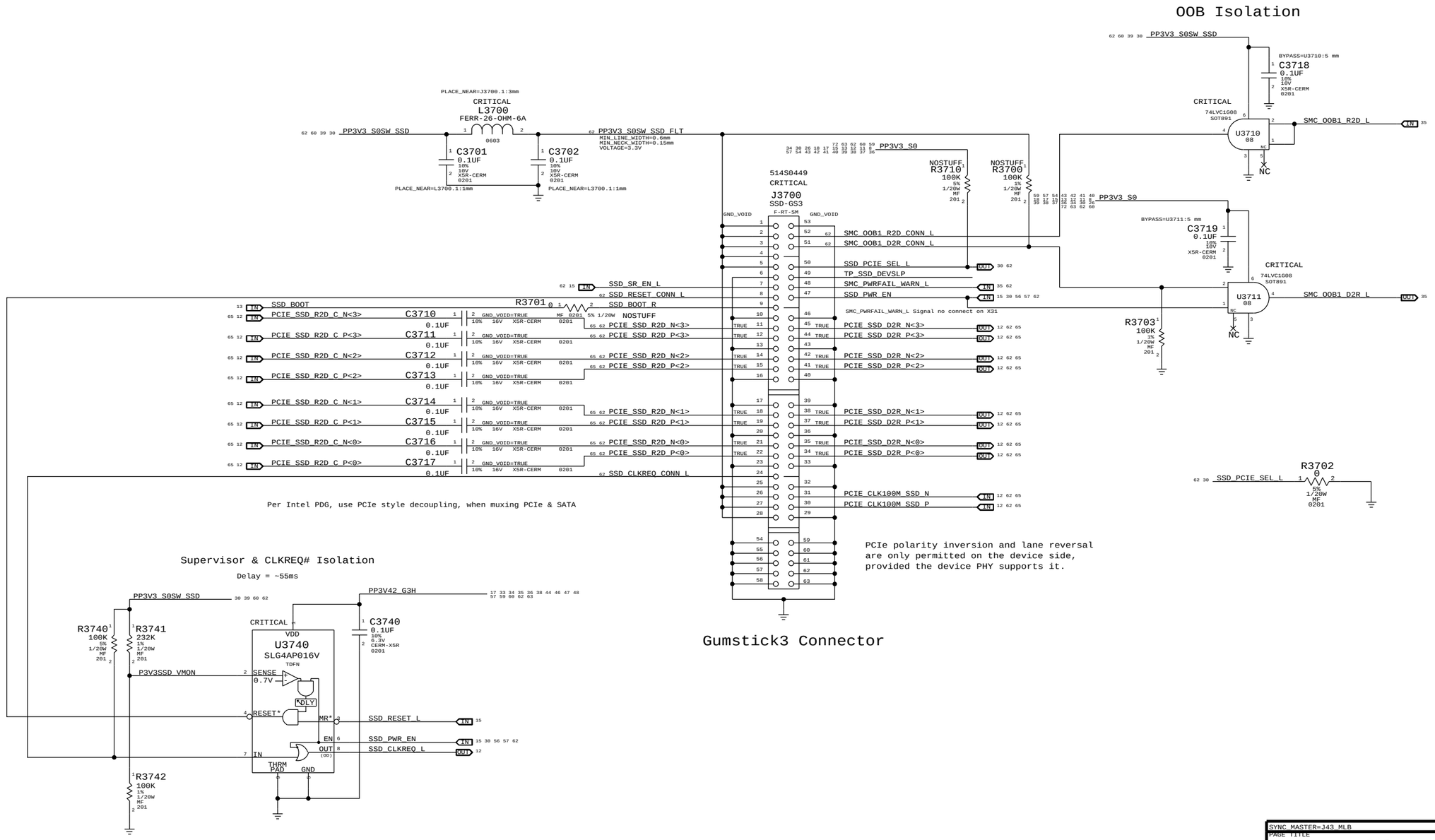
PAGE TITLE
Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 32 OF 120
SHEET 28 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


3.3V WLAN Switch
Part | TPS22924C
Type | Load Switch
R(on) @ 2.5V | 18.5 mOhm Typ 25.8 mOhm Max
Sense resistor on sensor page
PP3V3_WLAN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
PP3V3_WLAN_R
Max Current = 2A (85C)
U3550
TPS22924
CSP
VOUT
VIN
CRITICAL
ON
GND
PP3V3_S5
SMC_WIFI_PWR_EN
C3550
1.0UF
20%
6.3V
X5R
0201-1
C3521
0.1UF
10%
6.3V
CERM-X5R
0201
BYPASS=J3501:5mm
514S0335
CRITICAL
J3501
SSD-K99
F-RT-SM1
AIRPORT
WIFI_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_P
C3531
0.1UF
C3530
0.1UF
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PP3V3_S4
C3532
0.1UF
BYPASS=J3501:1.5mm
Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%
APCLKRQ:ISOL
R3553
100K
R3554
232K
P3V3WLAN_VMON
U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
DLY
RESET*
MR*
EN
OUT
IN
THRM PAD
GND
C3540
0.1UF
R3558
0
AP_RESET_CONN_L
AP_RESET_CONN_R_L
AP_RESET_L
SMC_WIFI_PWR_EN
AP_CLKREQ_Q_L
AP_CLKREQ_R_L
R3555
100K
APCLKRQ:ISOL
R3556
APCLKRQ:BIDIR
R3557
AP_CLKREQ_L
NOSTUFF
R3559
PCIe Wake Muxing
PP3V3_S5
R3561
100K
C3560
0.1UF
U3560
NC7SB3157P6XG
SC70
VER-3
VCC
GND
SEL | OUTPUT
L | PCIE_WAKE_L (B0)
H | AP_S0IX_WAKE_L (B1)
AP_S0IX_WAKE_SEL
PCIE_WAKE_L
AP_S0IX_WAKE_L
AP_PCIE_WAKE_L
NOSTUFF
R3560
BLUETOOTH
PP3V3_S4
C3510
0.1UF
U3510
USB3740
DFN
CRITICAL
VDD
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
USB_BT_P
USB_BT_N
BT_WAKE
PM_SLP_S4_L
USB_BT_CONN_P
USB_BT_CONN_N
SIGNAL_MODEL=BT_MUX
SEL | OUTPUT
L | BT_WAKE (1)
H | USB_BT (2)
SMC_PME_S4_WAKE_L
NO_XNET_CONNECTION=TRUE
Q3510
DMN32D2LFB4
R3512
15K
SYNC_MASTER=J43_MLB
SYNC_DATE=10/02/2012
PAGE TITLE
Wireless Connector
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
35 OF 120
SHEET
29 OF 73
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

SSD Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

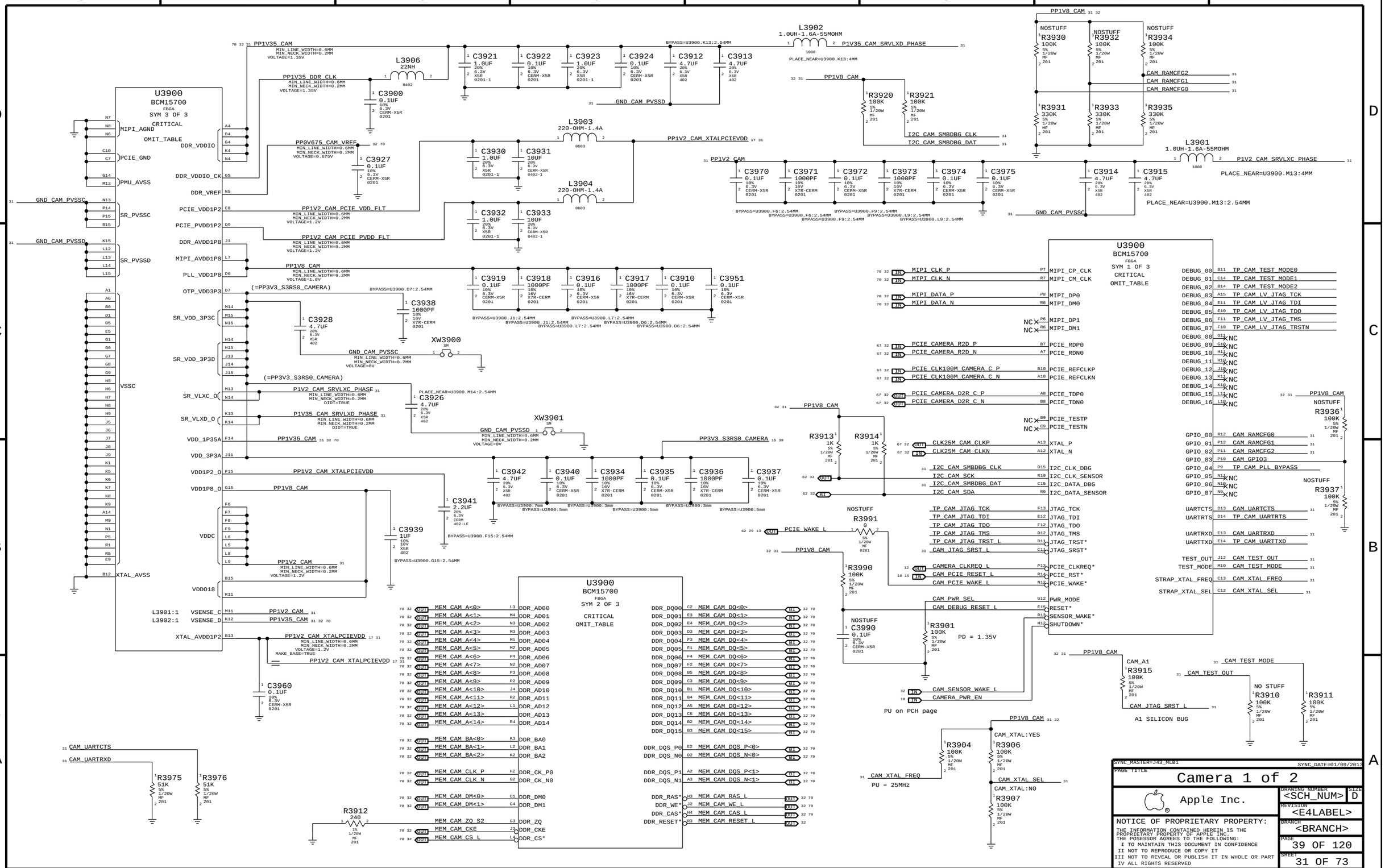
REVISION <E4LABEL>

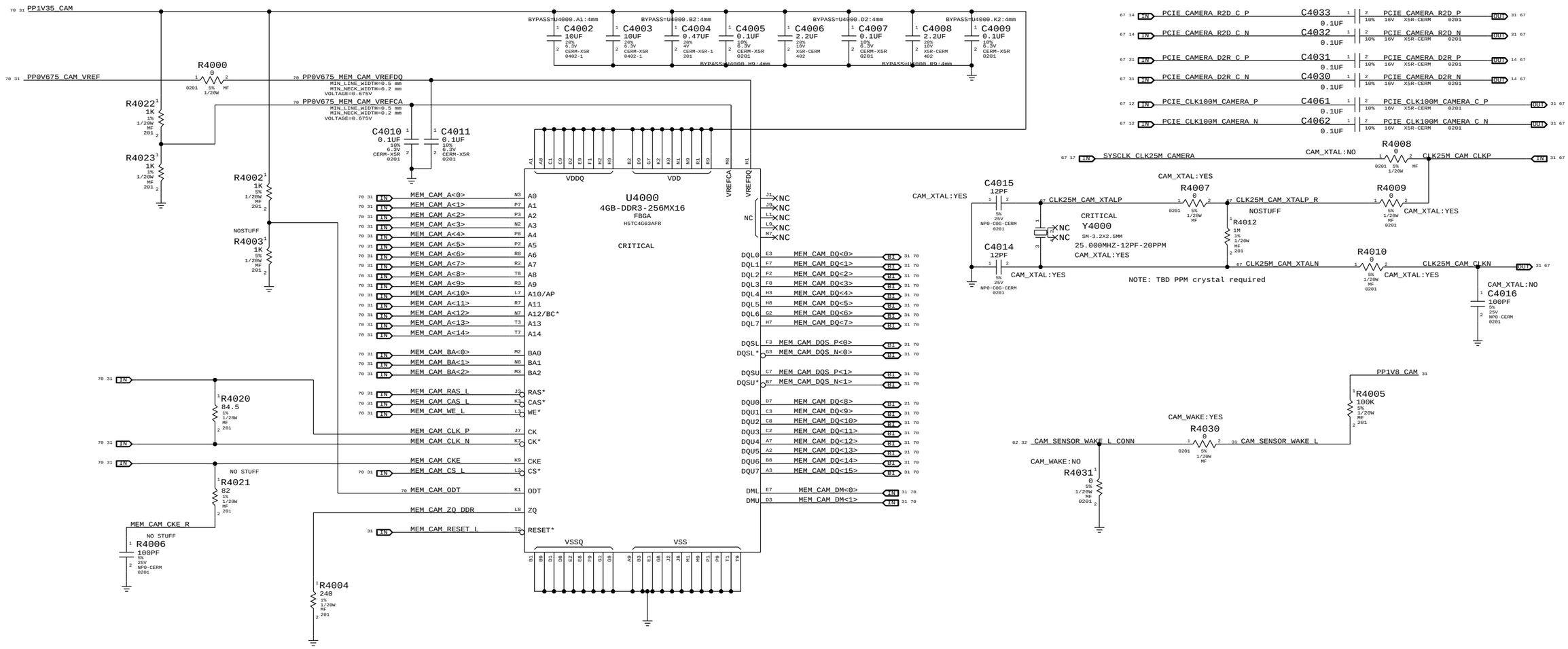
BRANCH <BRANCH>

PAGE 37 OF 120

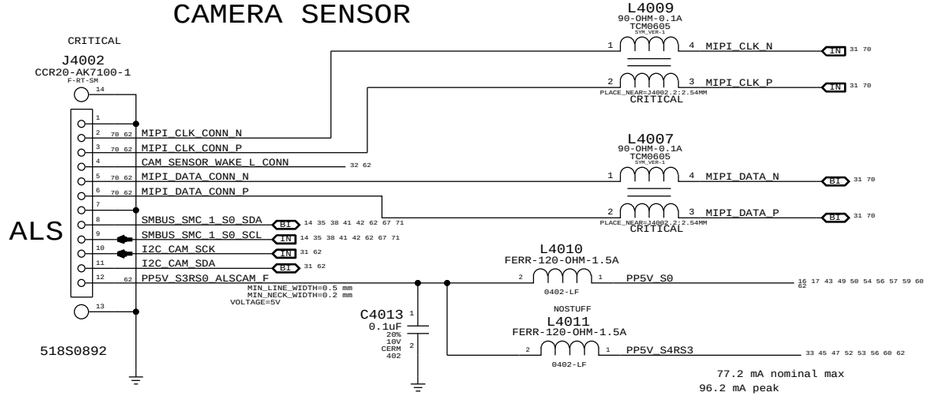
SHEET 30 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 2 OF 3
CRITICAL
OMIT_TABLE
L3902
1.0UH-1.6A-55MOHM
L3901
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP1V8_CAM
(=PP3V3_S3RS0_CAMERA)
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP1V35_CAM
PP1V2_CAM_XTALPCIEVDD
PP1V2_CAM
GND_CAM_PVSSC
GND_CAM_PVSSD
XW3900
XW3901
PP3V3_S3RS0_CAMERA
PCIE_WAKE_L
I2C_CAM_SMBDBG_CLK
I2C_CAM_SMBDBG_DAT
CAM_RAMCFG2
CAM_RAMCFG1
CAM_RAMCFG0
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAM_SENSOR_WAKE_L
CAMERA_PWR_EN
PU on PCH page
PD = 1.35V
CAM_XTAL_FREQ
PU = 25MHz
CAM_XTAL:YES
CAM_XTAL:NO
CAM_XTAL_SEL
CAM_A1
A1 SILICON BUG
CAM_TEST_MODE
CAM_TEST_OUT
NO STUFF
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_DQ<0>
MEM_CAM_DQ<1>
MEM_CAM_DQ<2>
MEM_CAM_DQ<3>
MEM_CAM_DQ<4>
MEM_CAM_DQ<5>
MEM_CAM_DQ<6>
MEM_CAM_DQ<7>
MEM_CAM_DQ<8>
MEM_CAM_DQ<9>
MEM_CAM_DQ<10>
MEM_CAM_DQ<11>
MEM_CAM_DQ<12>
MEM_CAM_DQ<13>
MEM_CAM_DQ<14>
MEM_CAM_DQ<15>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
DDR_AD00
DDR_AD01
DDR_AD02
DDR_AD03
DDR_AD04
DDR_AD05
DDR_AD06
DDR_AD07
DDR_AD08
DDR_AD09
DDR_AD10
DDR_AD11
DDR_AD12
DDR_AD13
DDR_AD14
DDR_BA0
DDR_BA1
DDR_BA2
DDR_CK_P0
DDR_CK_N0
DDR_DM0
DDR_DM1
DDR_ZQ
DDR_CKE
DDR_CS*
DDR_DQ00
DDR_DQ01
DDR_DQ02
DDR_DQ03
DDR_DQ04
DDR_DQ05
DDR_DQ06
DDR_DQ07
DDR_DQ08
DDR_DQ09
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQS_P0
DDR_DQS_N0
DDR_DQS_P1
DDR_DQS_N1
DDR_RAS*
DDR_WE*
DDR_CAS*
DDR_RESET*
MIPI_CP_CLK
MIPI_CM_CLK
MIPI_DP0
MIPI_DM0
MIPI_DP1
MIPI_DM1
PCIE_RDP0
PCIE_RDN0
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_TDP0
PCIE_TDN0
PCIE_TESTP
PCIE_TESTN
XTAL_P
XTAL_N
I2C_CLK_DBG
I2C_CLK_SENSOR
I2C_DATA_DBG
I2C_DATA_SENSOR
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*
JTAG_SRST*
PCIE_CLKREQ*
PCIE_RST*
PCIE_WAKE*
PWR_MODE
RESET*
SENSOR_WAKE*
SHUTDOWN*
TP_CAM_TEST_MODE0
TP_CAM_TEST_MODE1
TP_CAM_TEST_MODE2
TP_CAM_LV_JTAG_TCK
TP_CAM_LV_JTAG_TDI
TP_CAM_LV_JTAG_TDO
TP_CAM_LV_JTAG_TMS
TP_CAM_LV_JTAG_TRSTN
CAM_RAMCFG0
CAM_RAMCFG1
CAM_RAMCFG2
CAM_GPIO3
TP_CAM_PLL_BYPASS
CAM_UARTCTS
TP_CAM_UARTRTS
CAM_UARTRXD
TP_CAM_UARTTXD
CAM_TEST_OUT
CAM_TEST_MODE
CAM_XTAL_FREQ
CAM_XTAL_SEL
VSSC
VDDC
VDD018
XTAL_AVSS
XTAL_AVDD1P2
VSENSE_C
VSENSE_D
L3901:1
L3902:1
CAM_UARTCTS
CAM_UARTRXD
SYNC_MASTER=J43_MLB1
SYNC_DATE=01/09/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
39 OF 120
SHEET
31 OF 73
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



CAMERA SENSOR

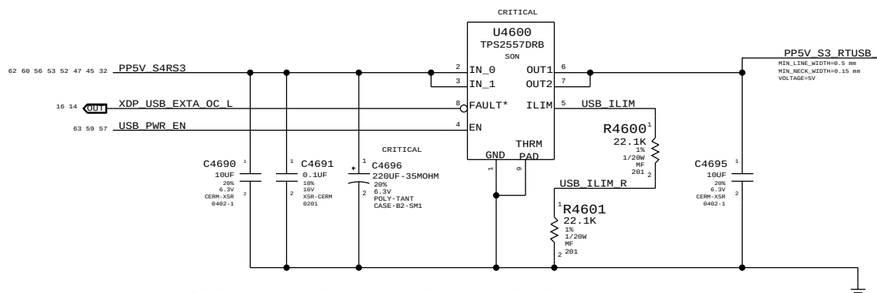


SYNC_MASTER=J43_MLB	SYNC_DATE=09/14/2012
PAGE TITLE	Camera 2 of 2
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 40 OF 120
	SHEET 32 OF 73

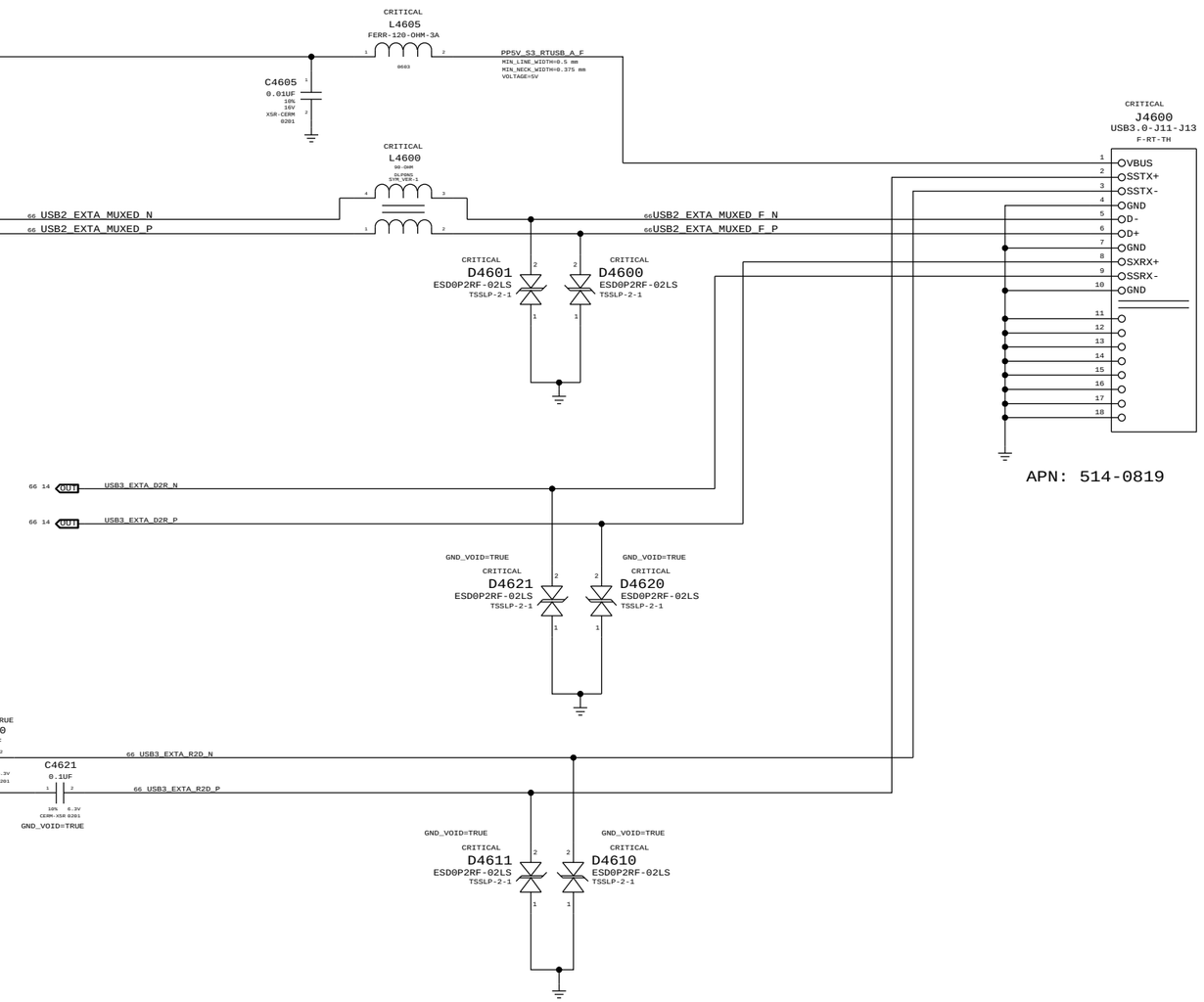
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Right USB Port A

USB Port Power Switch

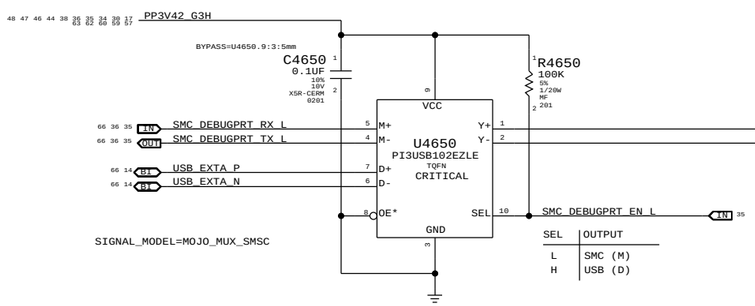


Current limit per port (R4600+R4601): 2.19A min / 2.76A max



APN: 514-0819

Mojo SMC Debug Mux



SEL	OUTPUT
L	SMC (M)
H	USB (D)

SYNC MASTER=J43_MLB SYNC DATE=02/20/2013

PAGE TITLE

External A USB3 Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

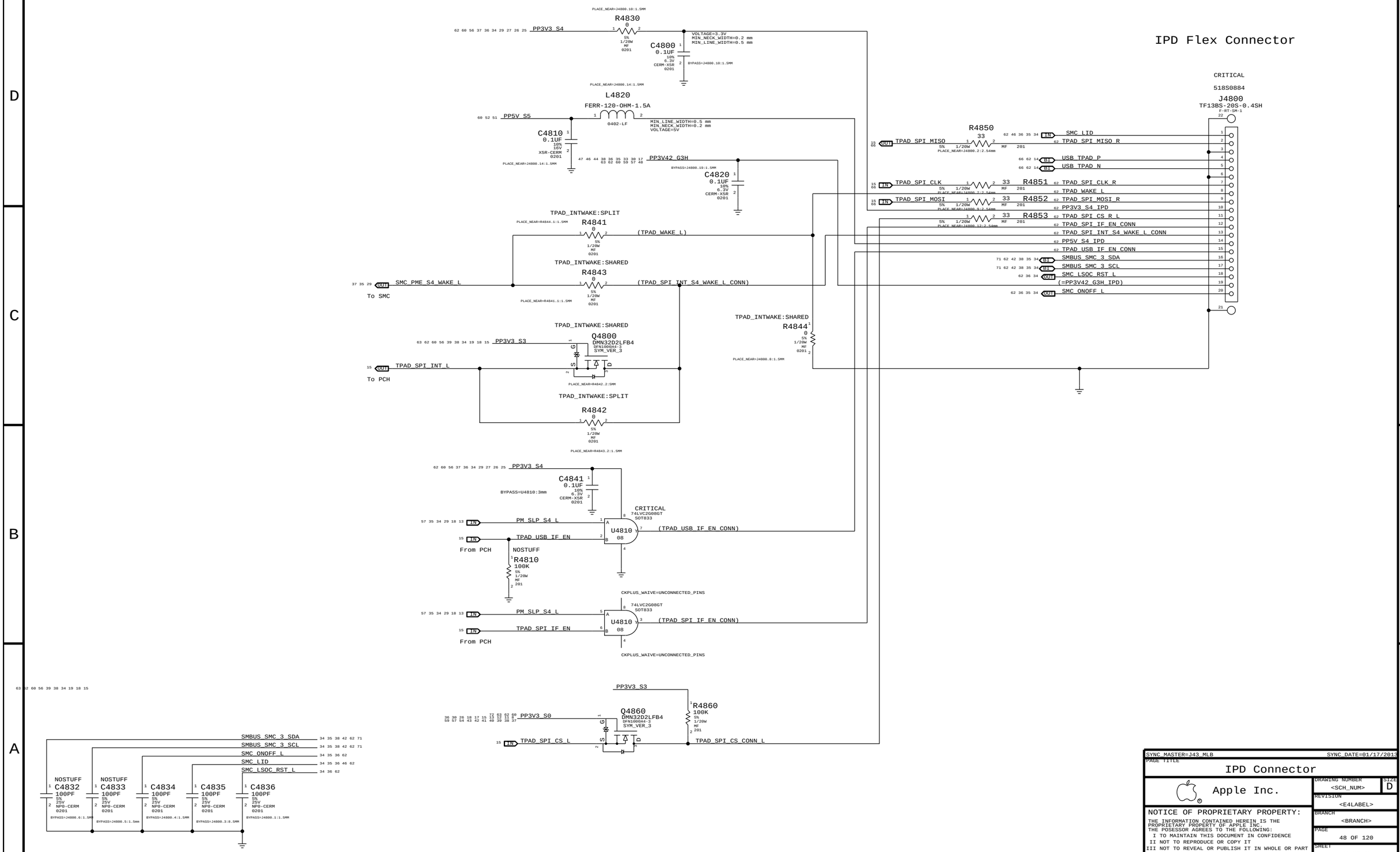
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 46 OF 120

SHEET 33 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE

IPD Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

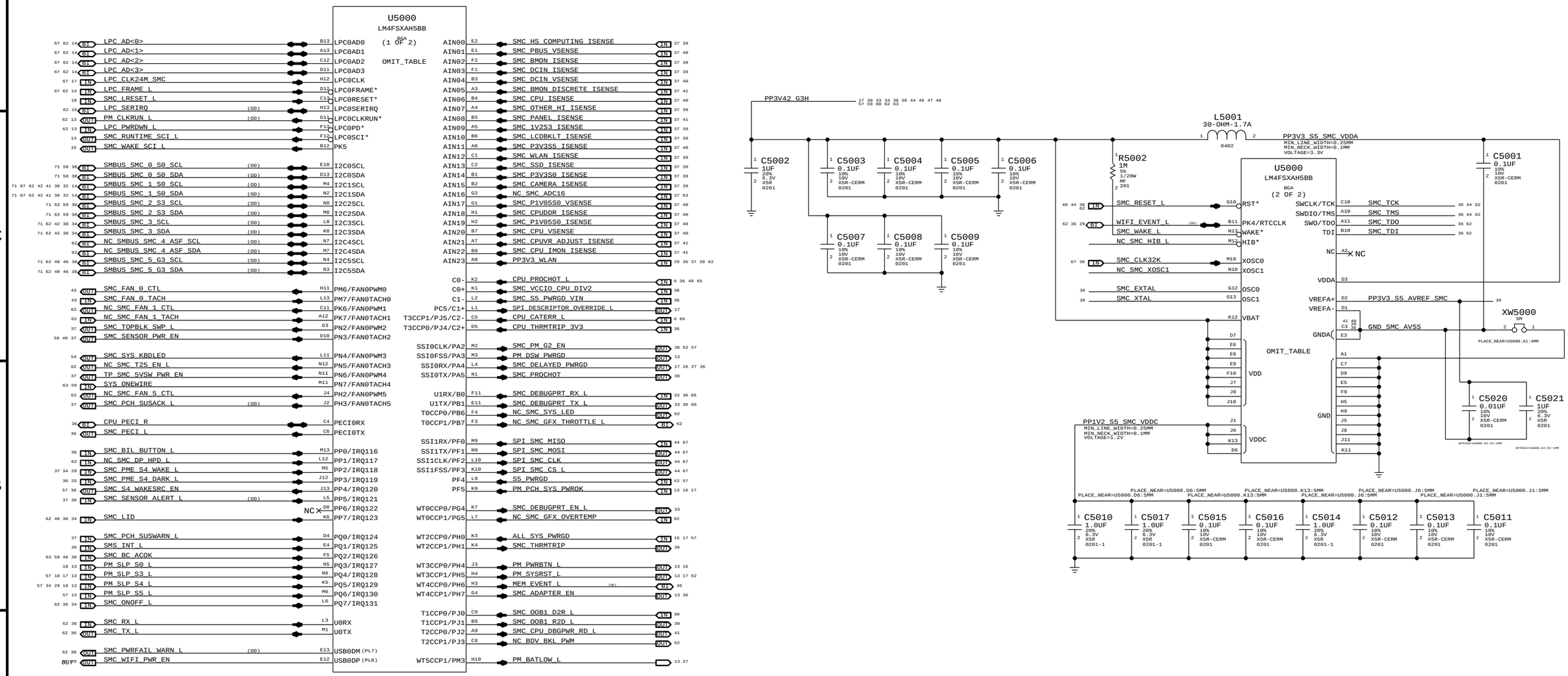
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 48 OF 120

SHEET 34 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=WILL_J43 SYNC_DATE=12/17/2012

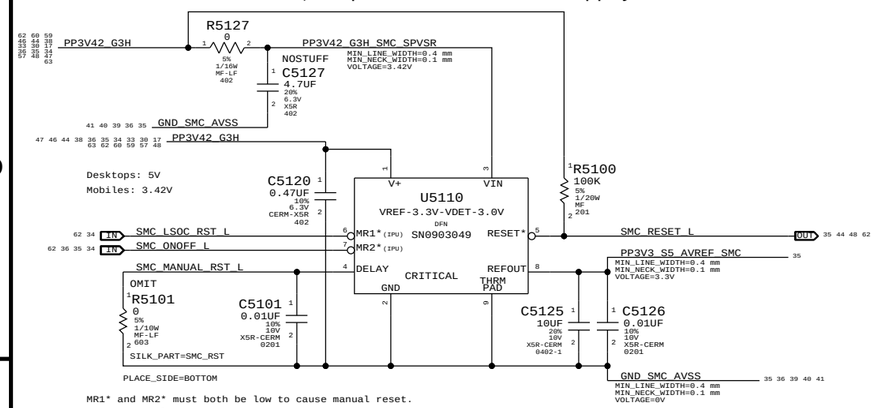
PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 50 OF 120
SHEET 35 OF 73

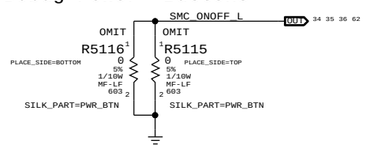
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SMC Reset "Button", Supervisor & AVREF Supply



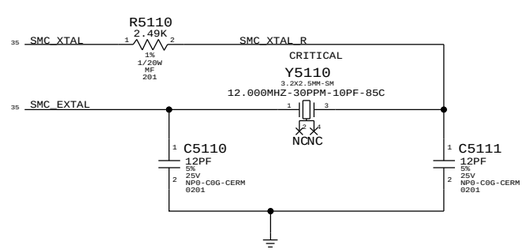
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

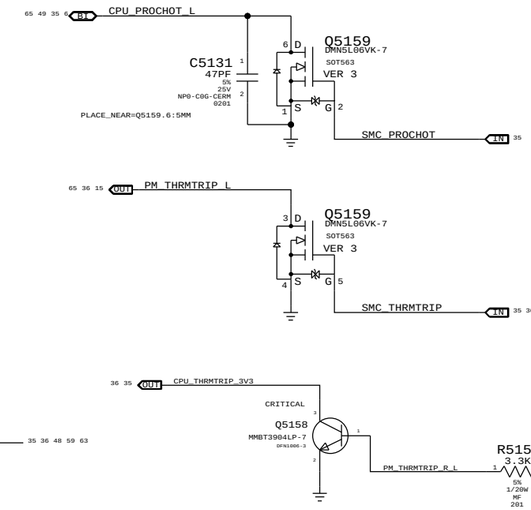
Debug Power "Buttons"



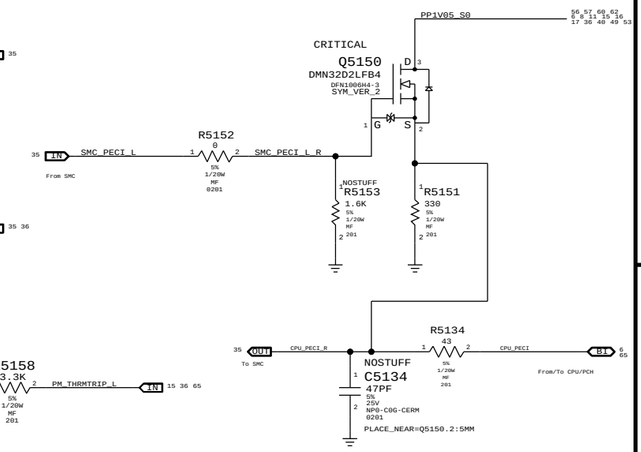
SMC Crystal Circuit

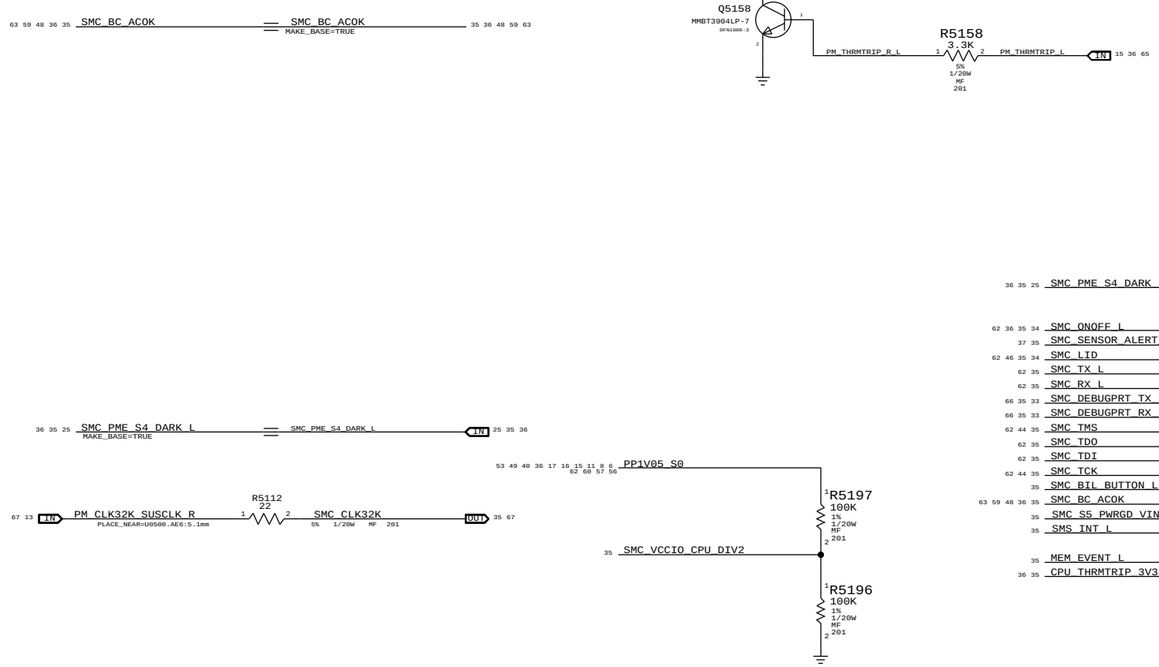
SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz

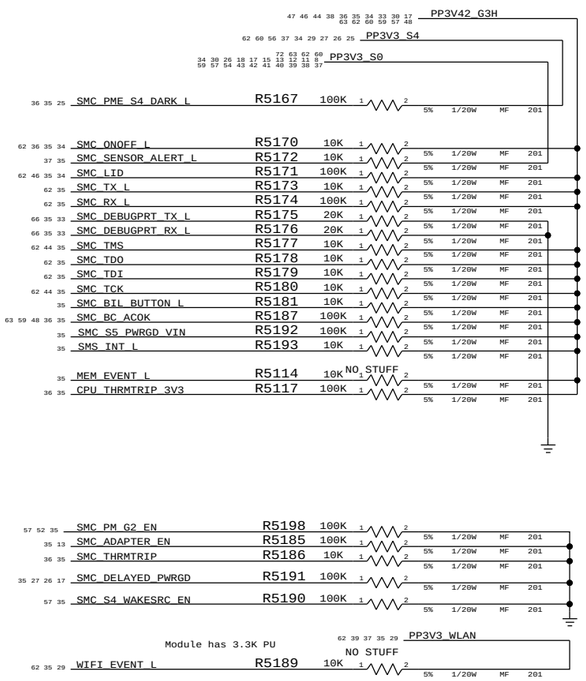




SMC12 PECI Support







SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

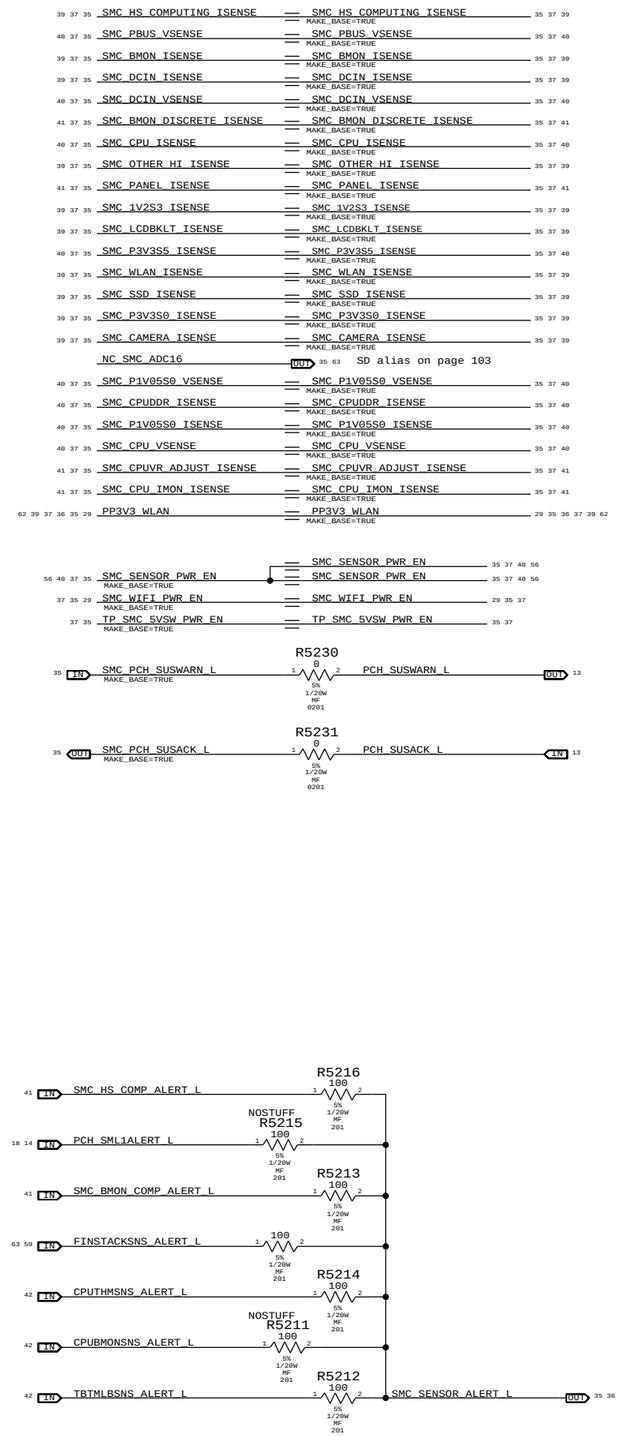
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 51 OF 120

SHEET: 36 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

SMC Project Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

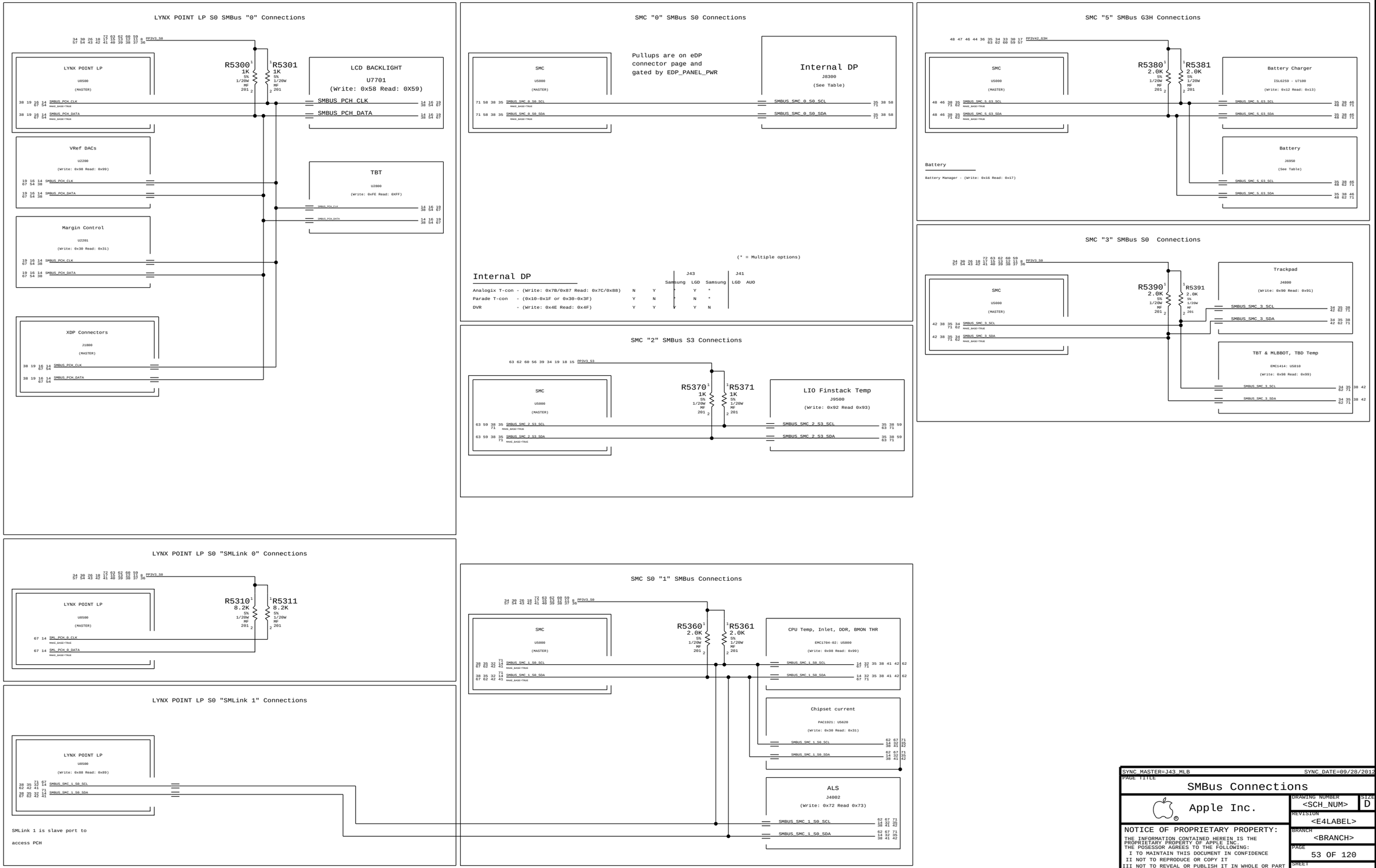
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 52 OF 120

SHEET 37 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB SYNC_DATE=09/28/2012

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

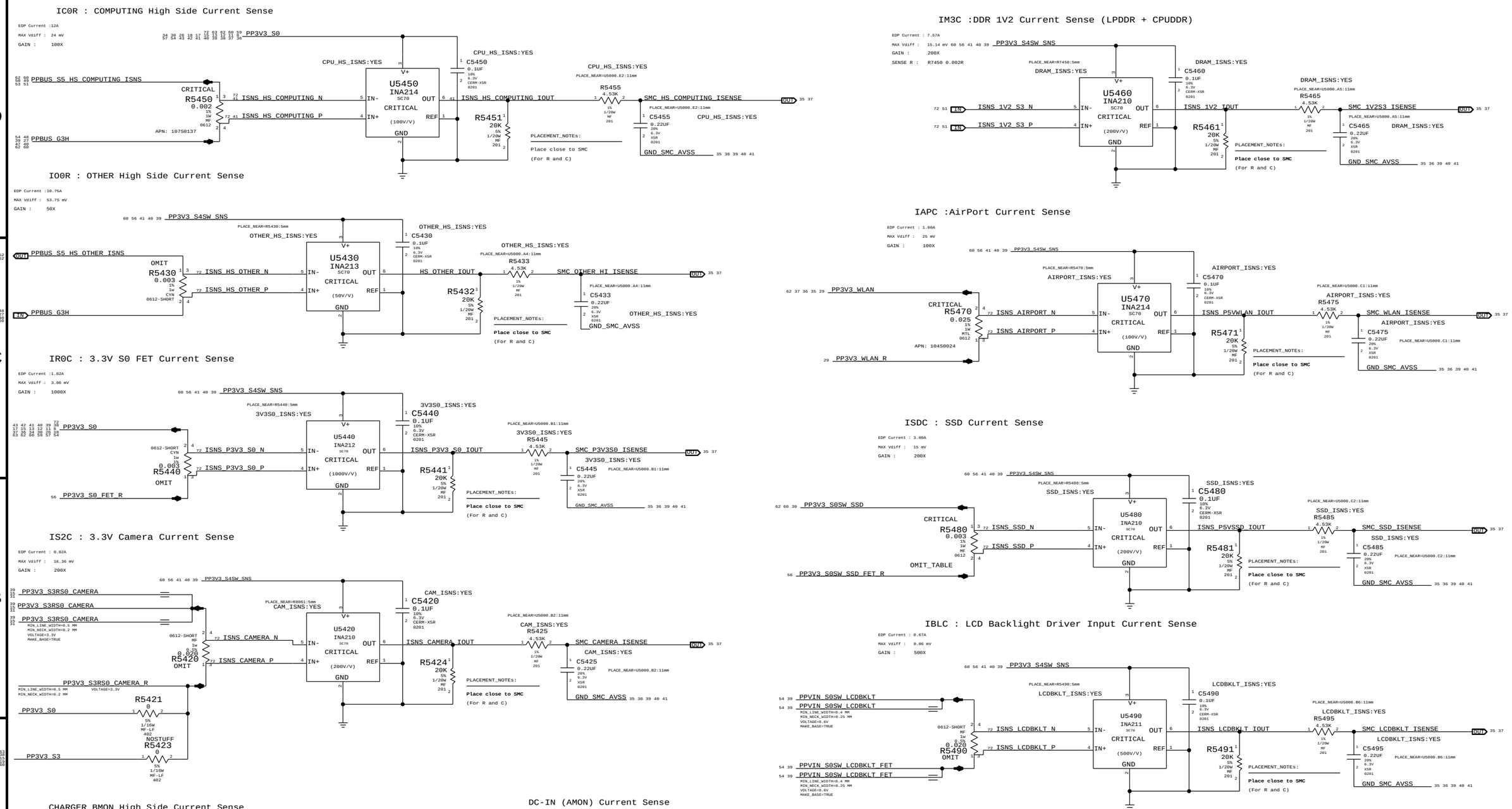
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 53 OF 120

SHEET 38 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.0030HM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE

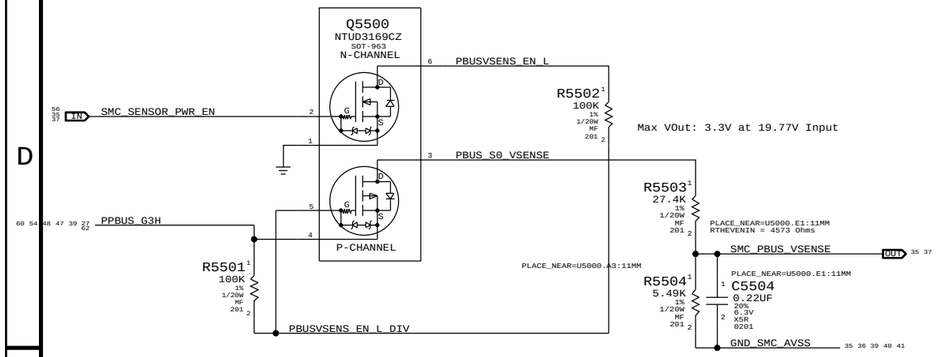
High Side Current Sensing

Apple Inc.

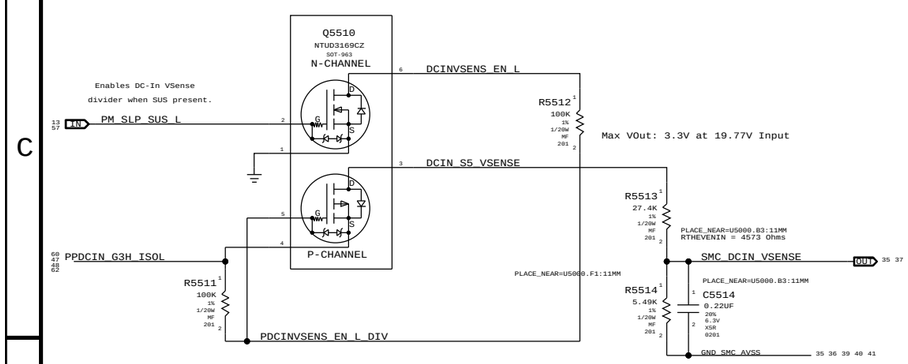
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	54 OF 120
SHEET	39 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

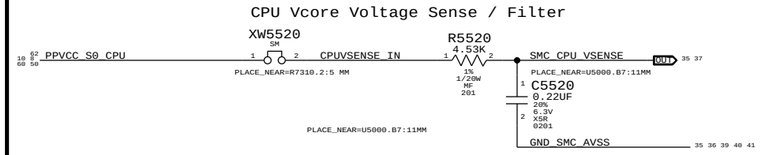
VP0R: PBUS Voltage Sense Enable & Filter



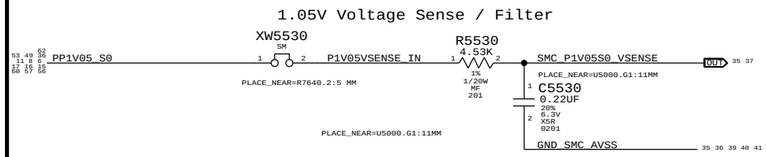
VD0R: DC-In Voltage Sense Enable & Filter



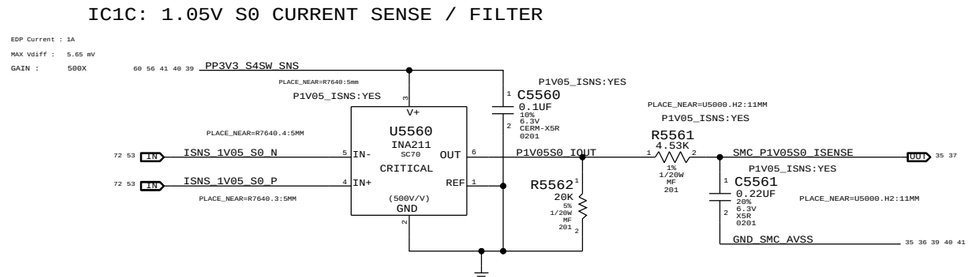
CPU Vcore Voltage Sense / Filter



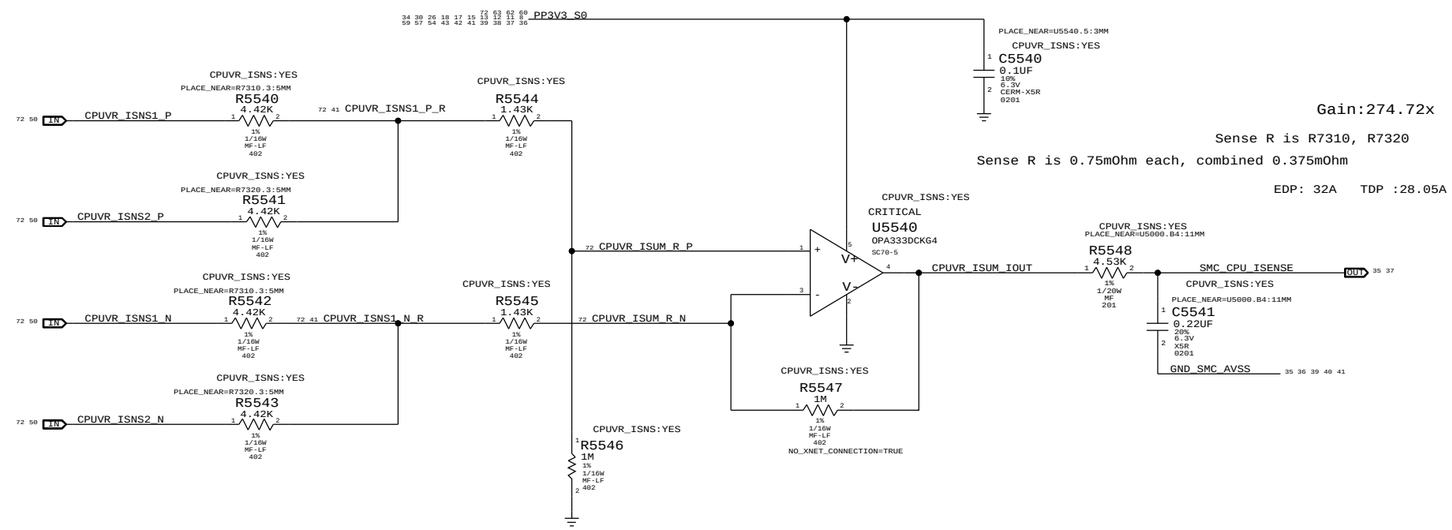
1.05V Voltage Sense / Filter



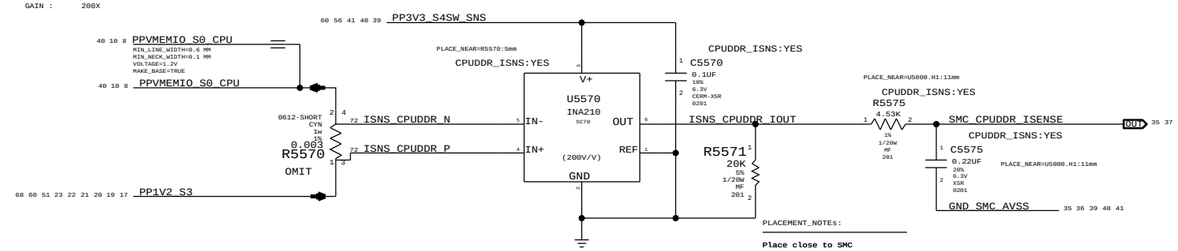
IC1C: 1.05V S0 CURRENT SENSE / FILTER



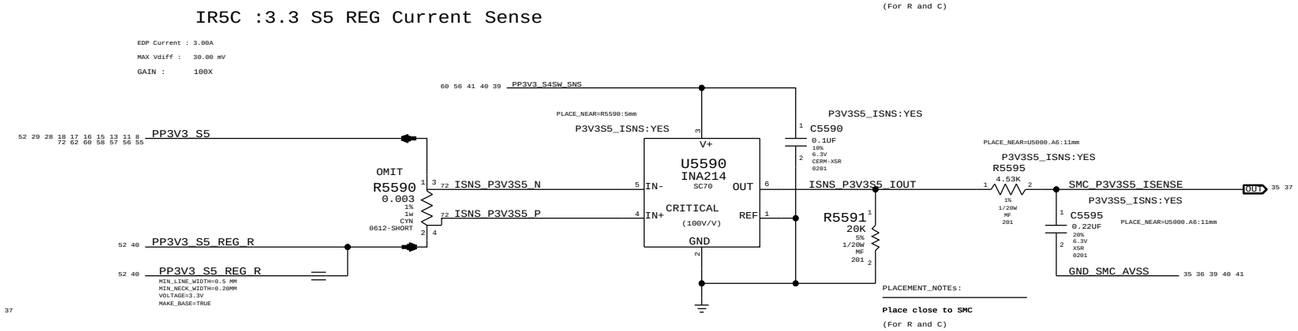
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C :3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE
Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

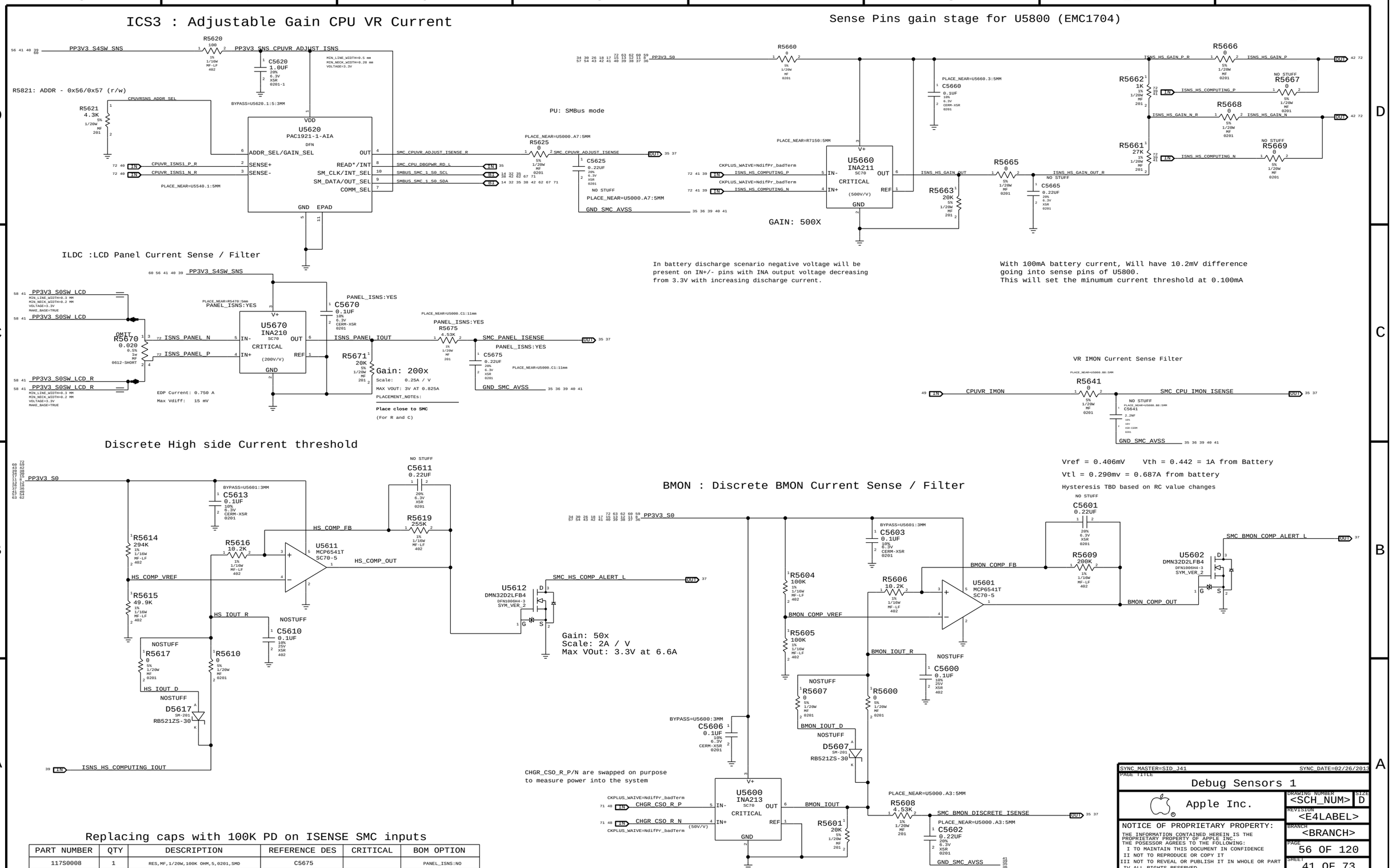
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 55 OF 120

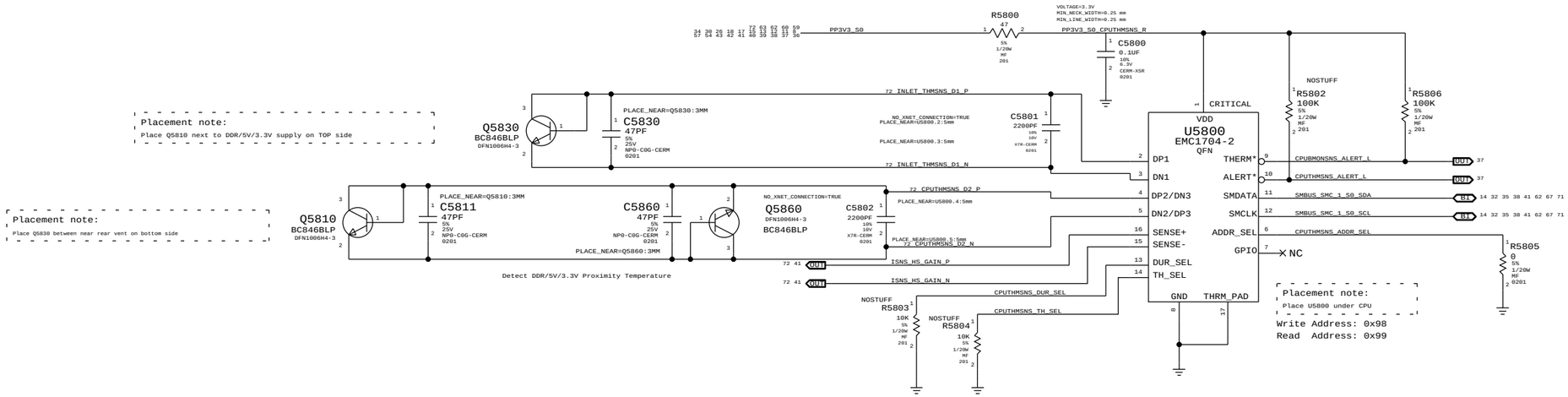
SHEET 40 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

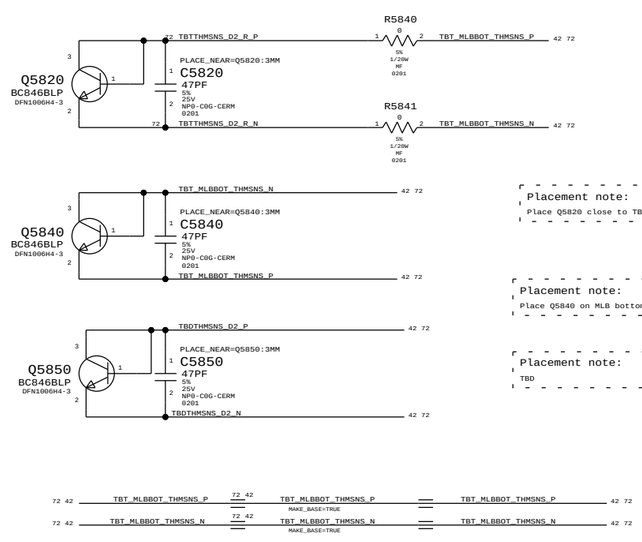


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

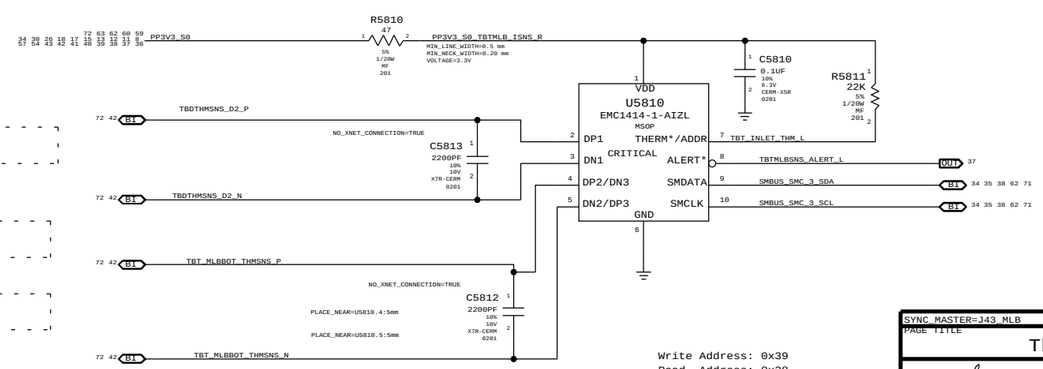
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors



TBT, MLBBOT and TBD Temp Sensor



SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

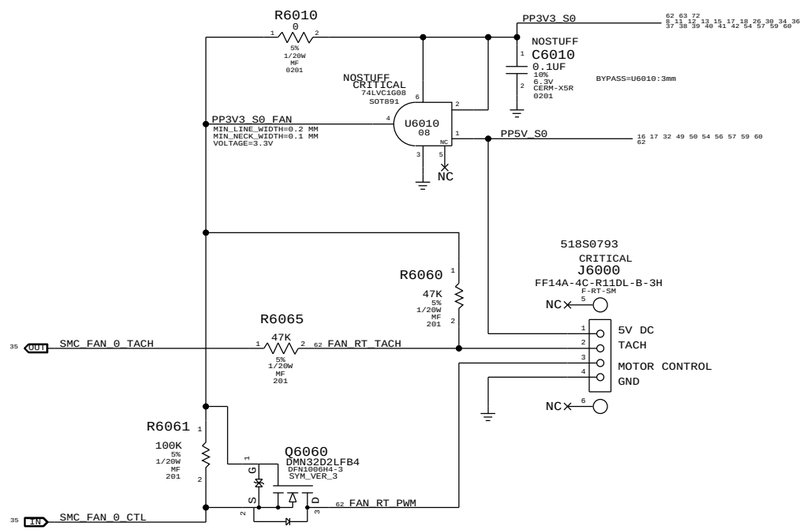
BRANCH <BRANCH>

PAGE 58 OF 120

SHEET 42 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

FAN CONNECTOR



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

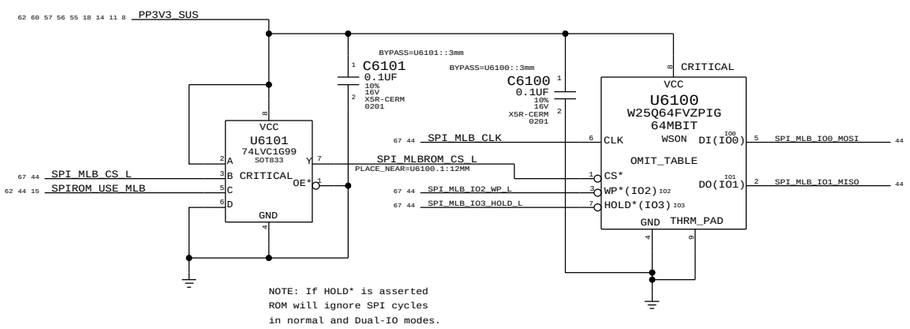
PAGE 60 OF 120

SHEET 43 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SPI ROM

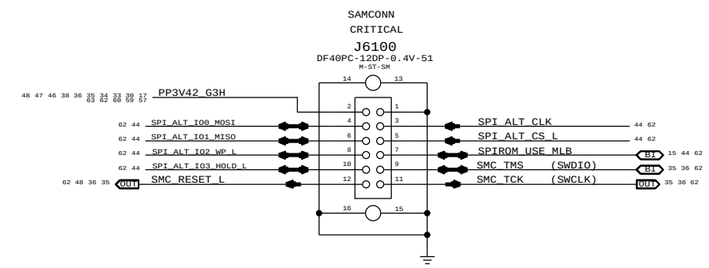
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



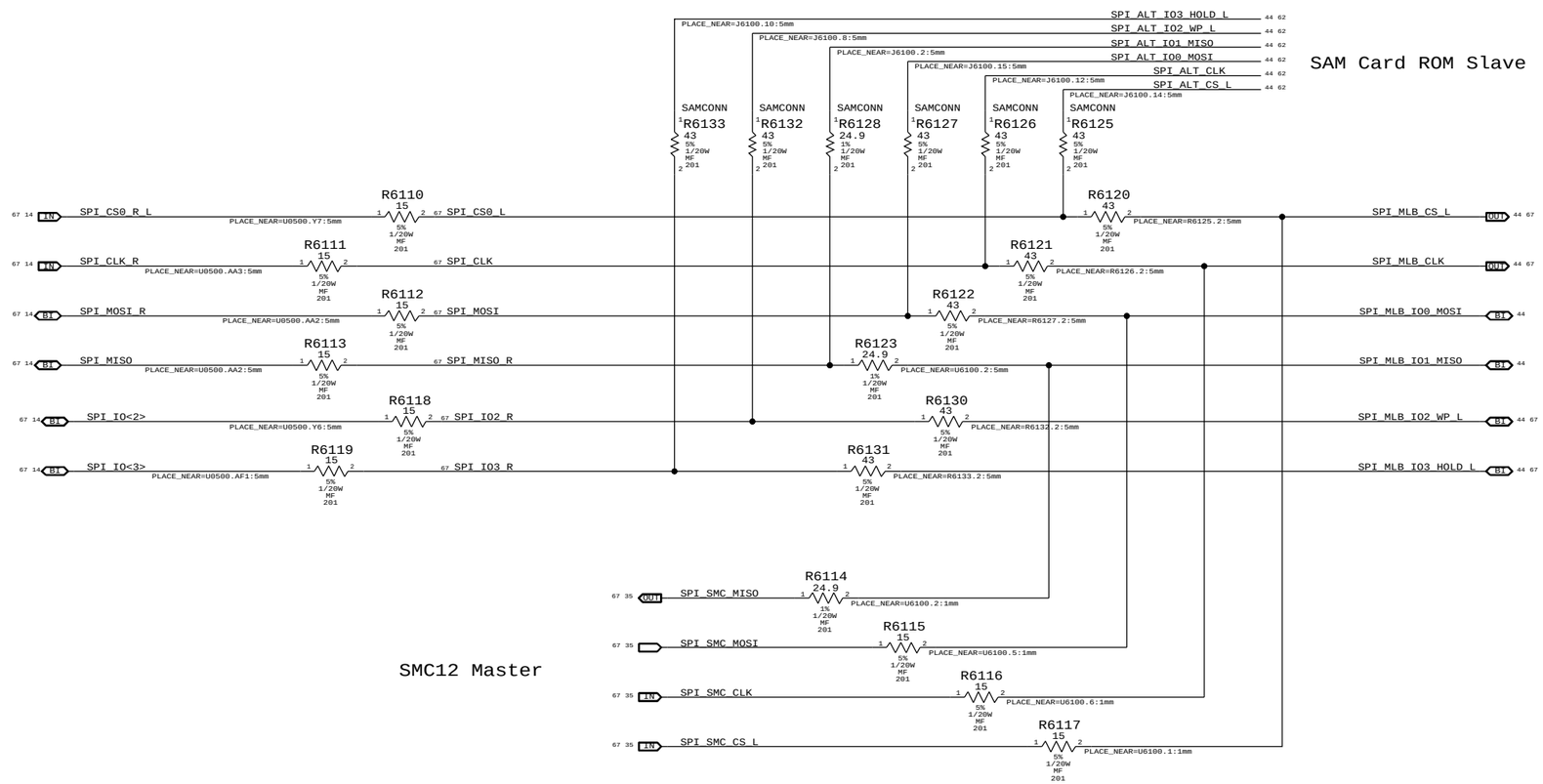
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination



SMC12 Master

IN

BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE
SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 61 OF 120
SHEET 44 OF 73

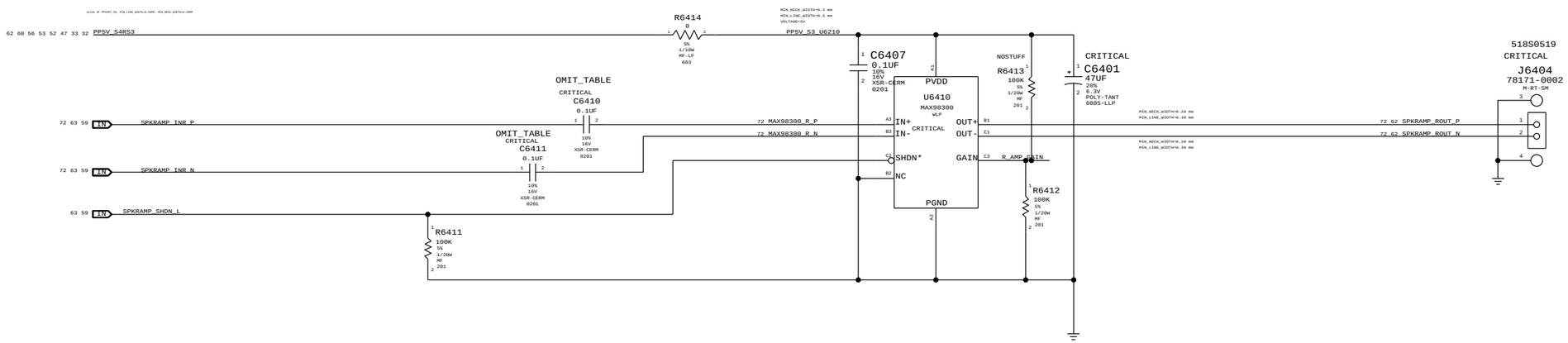
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB

Right Speaker Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0460	2	CAP,CER,X5R,0.1UF,10%,16V,0201,MURATA	C6410,C6411	CRITICAL	

SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE

Audio: Speaker Amp

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

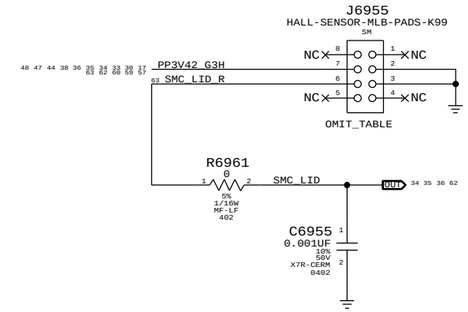
BRANCH <BRANCH>

PAGE 64 OF 120

SHEET 45 OF 73

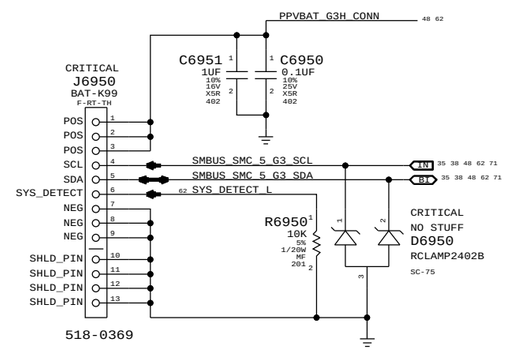
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Hall Effect Sensor



11"-Specific

Battery Connector



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Battery Connector & Hall Effect

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

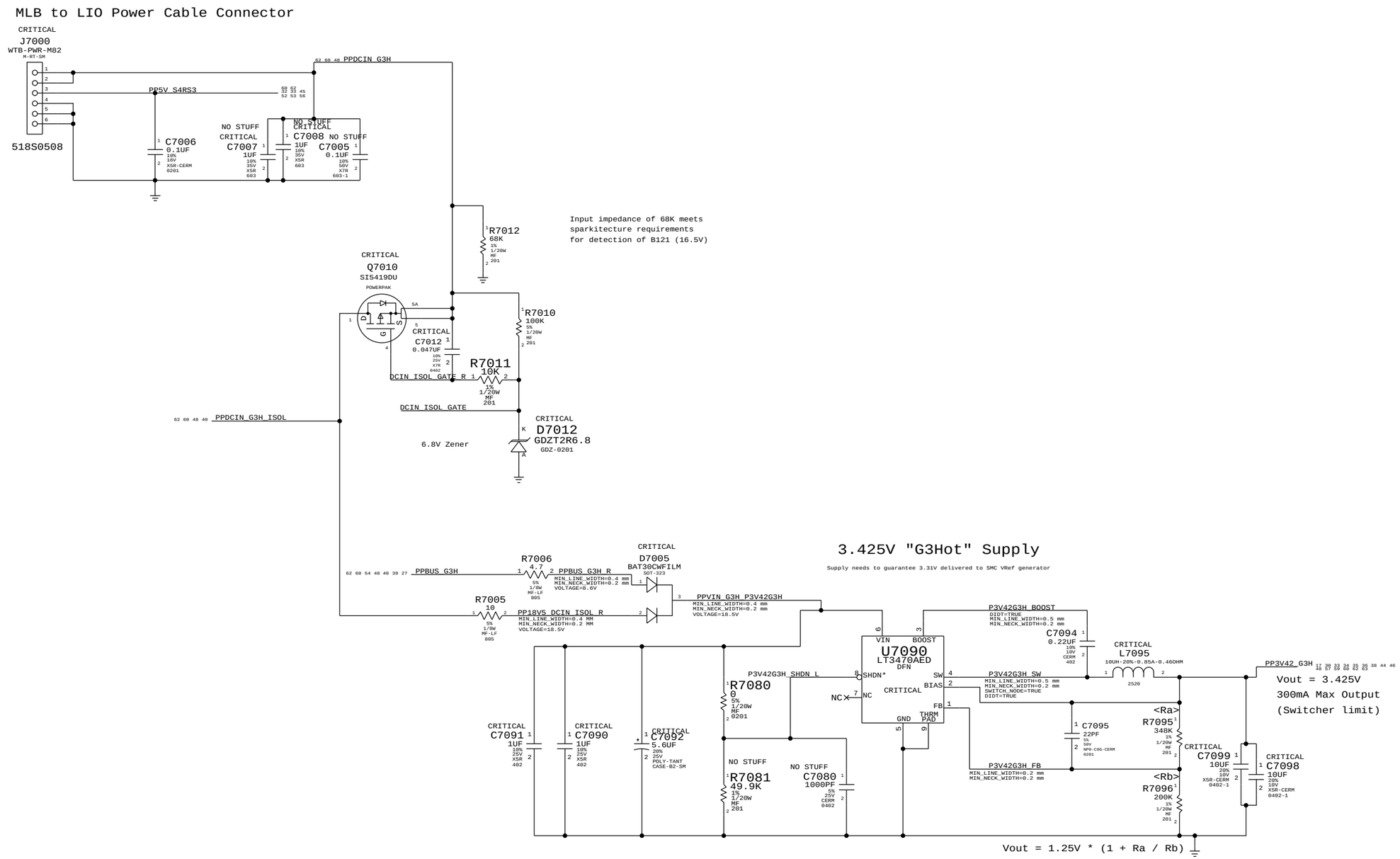
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 69 OF 120

SHEET 46 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE

DC-In & G3H Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

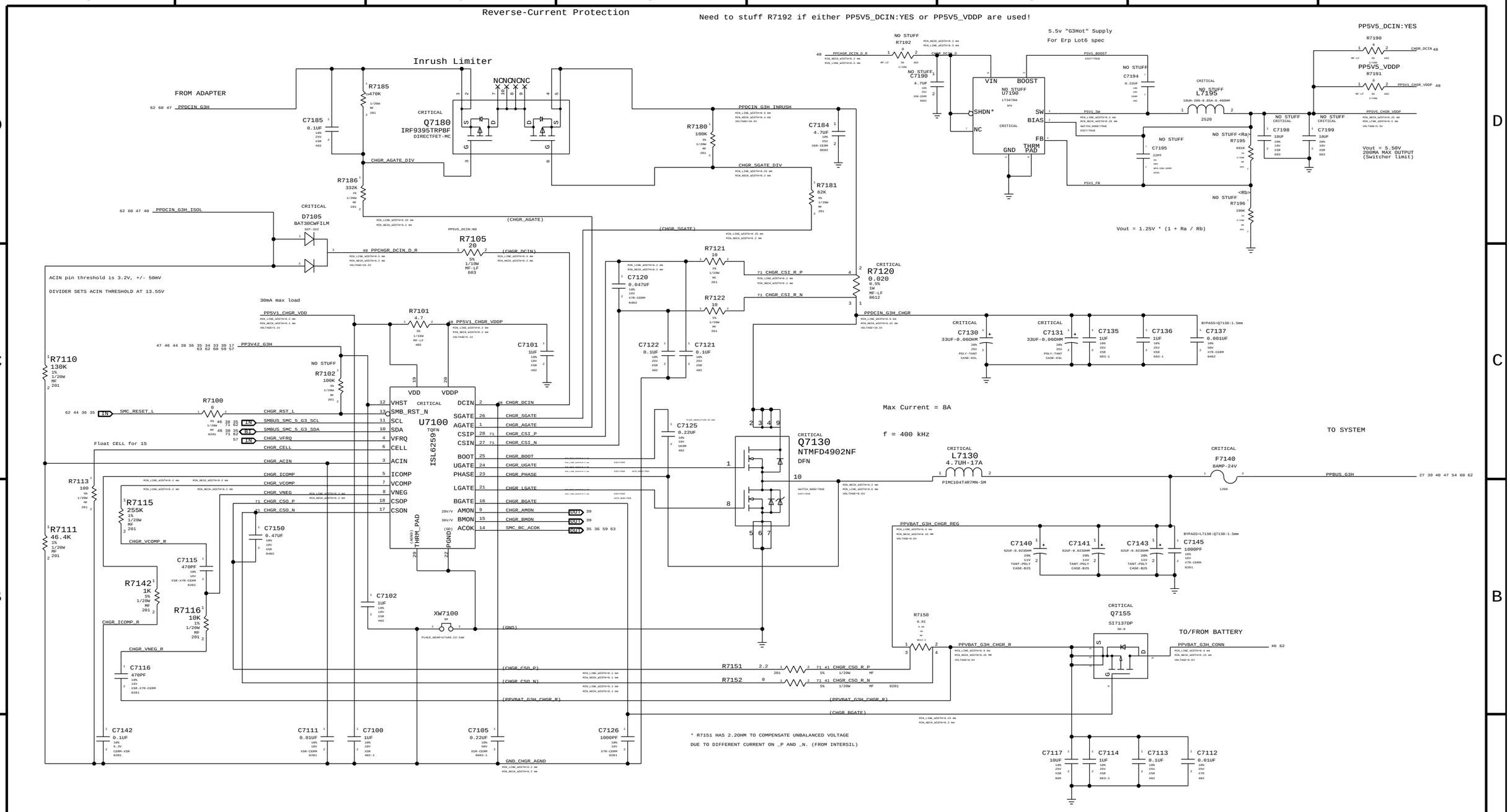
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 70 OF 120

SHEET 47 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=J43_MLB SYNC DATE=09/14/2012

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

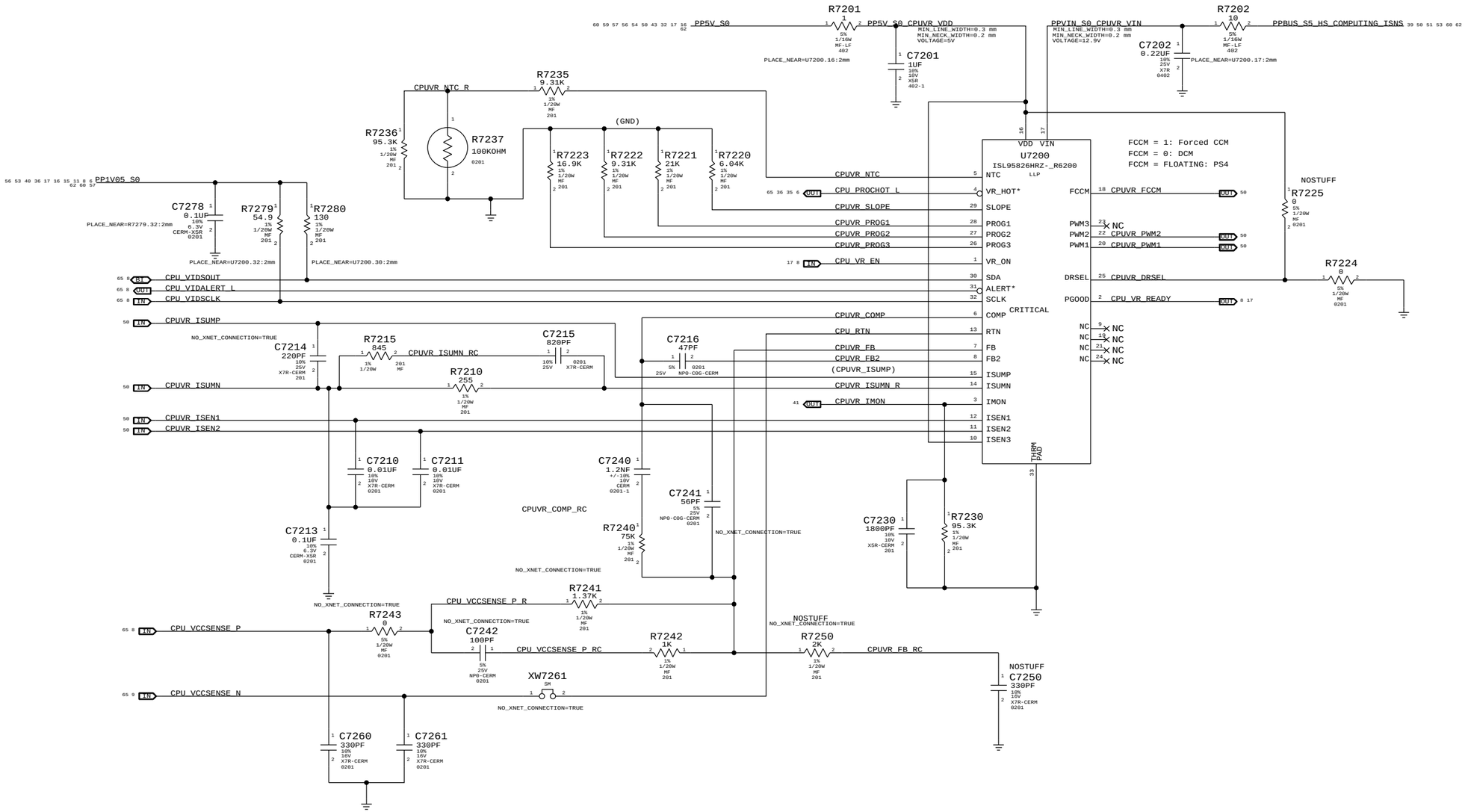
REVISION <E4LABEL>

BRANCH <BRANCH>

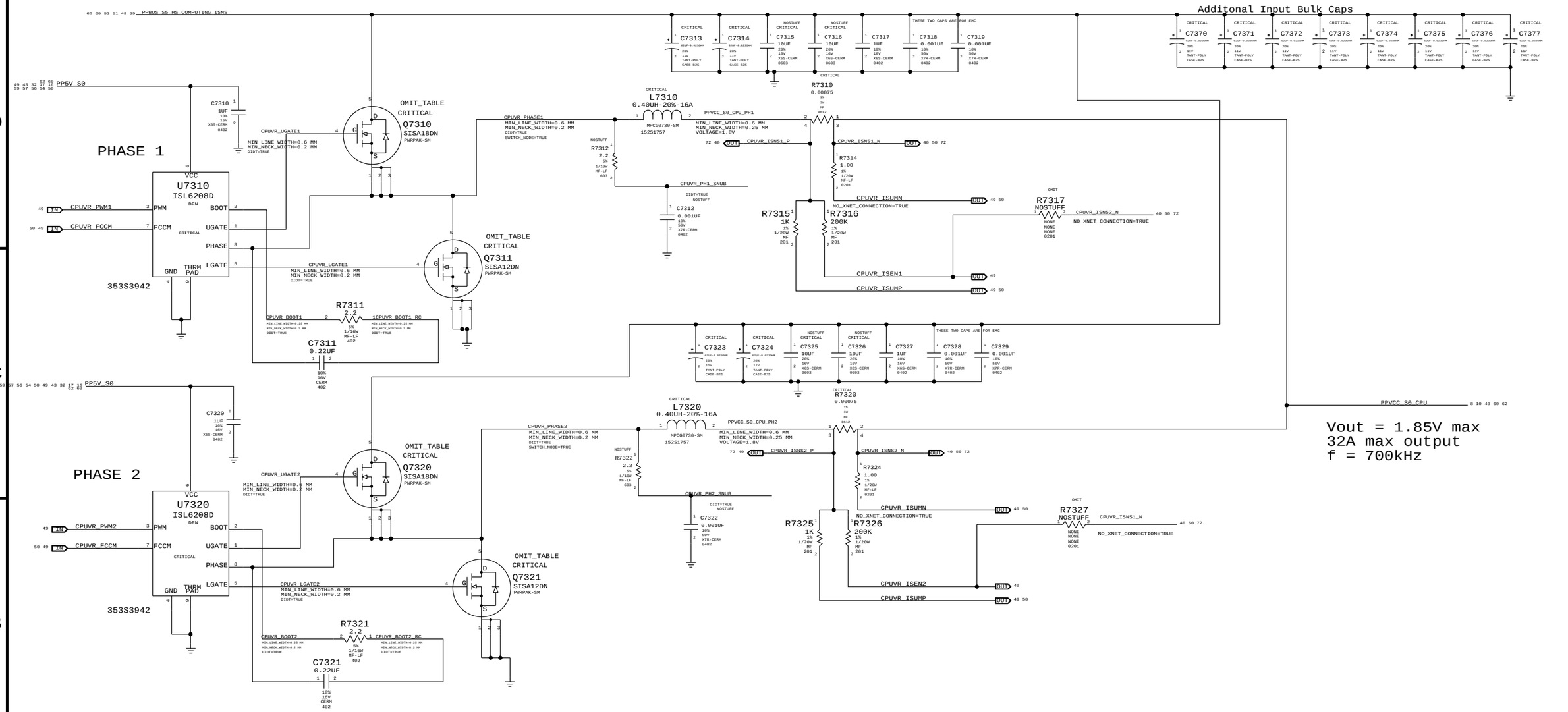
PAGE 71 OF 120

SHEET 48 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB	SYNC_DATE=10/09/2012
PAGE TITLE	CPU VR12.6 VCC Regulator IC
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH <BRANCH>
	PAGE 72 OF 120
	SHEET 49 OF 73



SYNC MASTER=J43_MLB SYNC DATE=09/21/2012

PAGE TITLE

CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

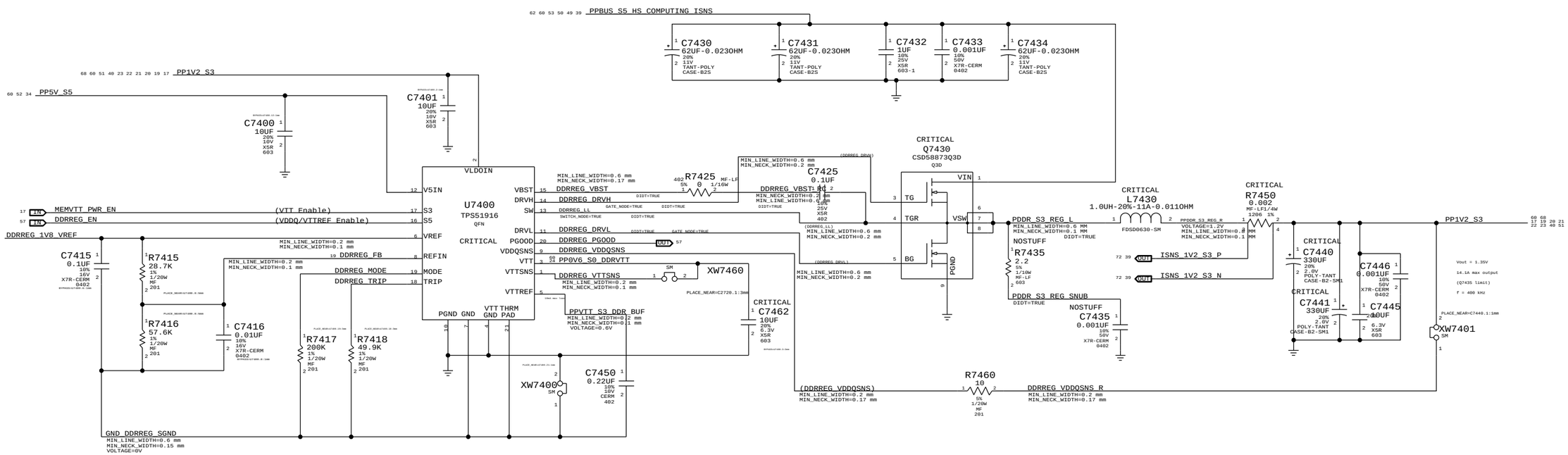
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 73 OF 120

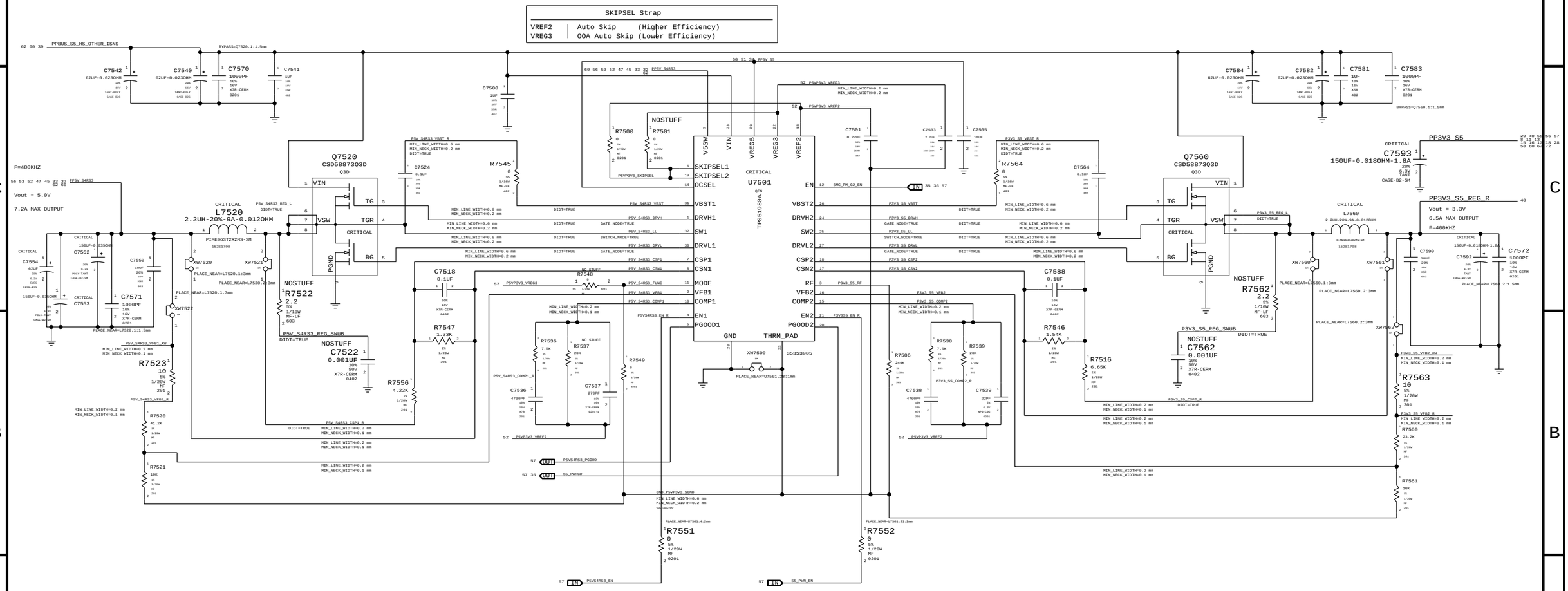
SHEET 50 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB	SYNC_DATE=09/17/2012
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 74 OF 120
	SHEET 51 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=J43_MLB SYNC DATE=10/02/2012

PAGE TITLE

5V S4RS3 / 3.3V S5 Power Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM>

SIZE: D

REVISION: <E4LABEL>

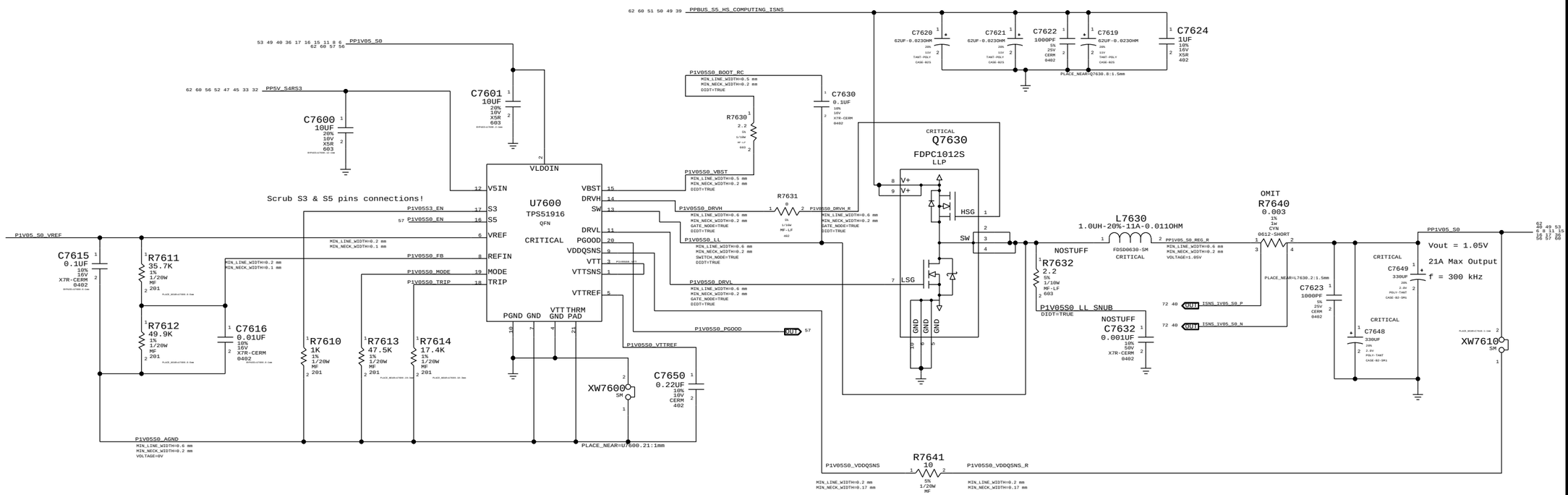
BRANCH: <BRANCH>

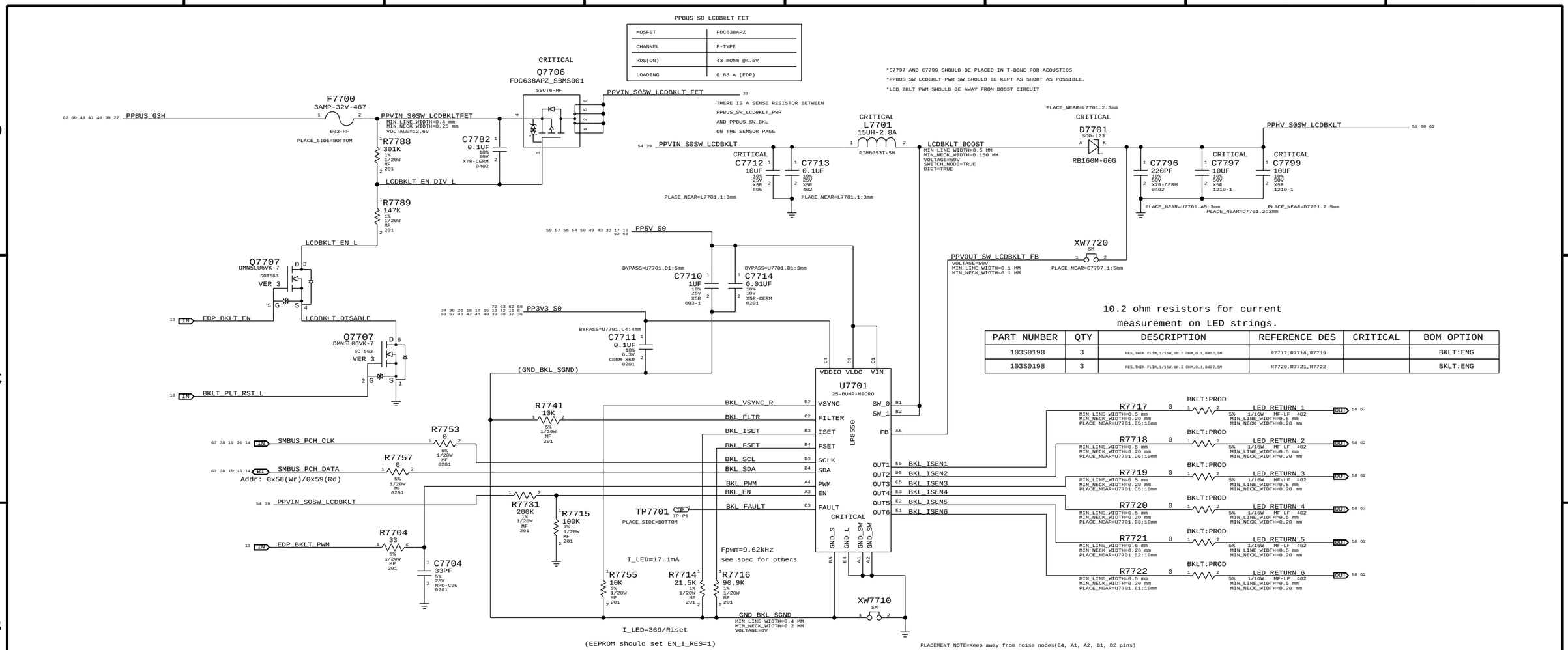
PAGE: 75 OF 120

SHEET: 52 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.05V S0 Regulator

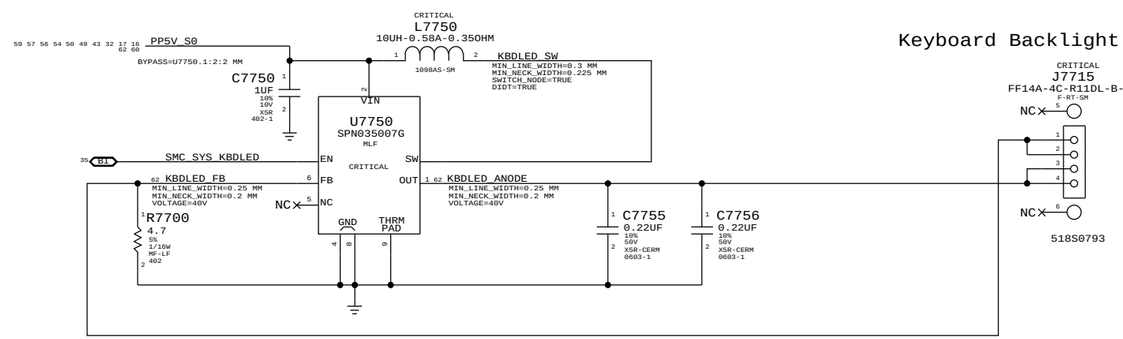

U7600
TPS51916
QFN
CRITICAL
Q7630
FDPC1012S
LLP
L7630
1.0UH-20%-11A-0.0110HM
FDSD0630-SM
CRITICAL
OMIT
R7640
0.003
1%
1W
CYN
0612-SHORT
Vout = 1.05V
21A Max Output
f = 300 kHz
Scrub S3 & S5 pins connections!
PP1V05_S0
PP5V_S4RS3
PPBUS_S5_HS_COMPUTING_ISNS
VLDOIN
V5IN
S3
S5
VREF
REFIN
MODE
TRIP
VBST
DRVH
SW
DRVL
PGOOD
VDDQSNS
VTT
VTTSNS
VTTREF
VTT THRM GND PAD
PGND GND
HSG
LSG
V+
GND
NOSTUFF
R7632
2.2
5%
1/10W
MF-LF
603
NOSTUFF
C7632
0.001UF
10%
50V
X7R-CERM
0402
P1V05S0_LL_SNUB
DIDT=TRUE
R7641
10
5%
1/20W
MF
201
P1V05S0_VDDQSNS
P1V05S0_VDDQSNS_R
P1V05S0_AGND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V
PLACE_NEAR=U7600.21:1mm
XW7600
XW7610
C7615
0.1UF
10%
16V
X7R-CERM
0402
C7616
0.01UF
10%
16V
X7R-CERM
0402
C7600
10UF
20%
10V
X5R
603
C7601
10UF
20%
10V
X5R
603
C7650
0.22UF
10%
10V
CERM
402
C7620
62UF-0.0230HM
C7621
62UF-0.0230HM
C7622
1000PF
5%
25V
CERM
0402
C7619
62UF-0.0230HM
C7624
1UF
10%
16V
X5R
402
C7630
0.1UF
10%
16V
X7R-CERM
0402
R7630
2.2
5%
1/10W
MF-LF
603
R7631
0
5%
1/16W
MF-LF
402
R7610
1K
1%
1/20W
MF
201
R7611
35.7K
1%
1/20W
MF
201
R7612
49.9K
1%
1/20W
MF
201
R7613
47.5K
1%
1/20W
MF
201
R7614
17.4K
1%
1/20W
MF
201
C7623
1000PF
5%
25V
CERM
0402
C7648
330UF
20%
2.4V
POLY-TANT
CASE-B2-SMT
C7649
330UF
20%
2.4V
POLY-TANT
CASE-B2-SMT
P1V05S0_BOOT_RC
P1V05S0_VBST
P1V05S0_DRVH
P1V05S0_DRVH_R
P1V05S0_LL
P1V05S0_DRVL
P1V05S0_PGOOD
P1V05S0_VTTREF
P1V05S3_EN
P1V05S0_EN
P1V05S0_FB
P1V05S0_MODE
P1V05S0_TRIP
P1V05S0_SW
P1V05S0_SW_R
P1V05S0_SW_RC
P1V05S0_SW_RCC
P1V05S0_SW_RCCC
P1V05S0_SW_RCCCC
P1V05S0_SW_RCCCCC
P1V05S0_SW_RCCCCCC
P1V05S0_SW_RCCCCCCC
P1V05S0_SW_RCCCCCCCC
P1V05S0_SW_RCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
P1V05S0_SW_RC



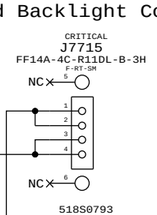
10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE: LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

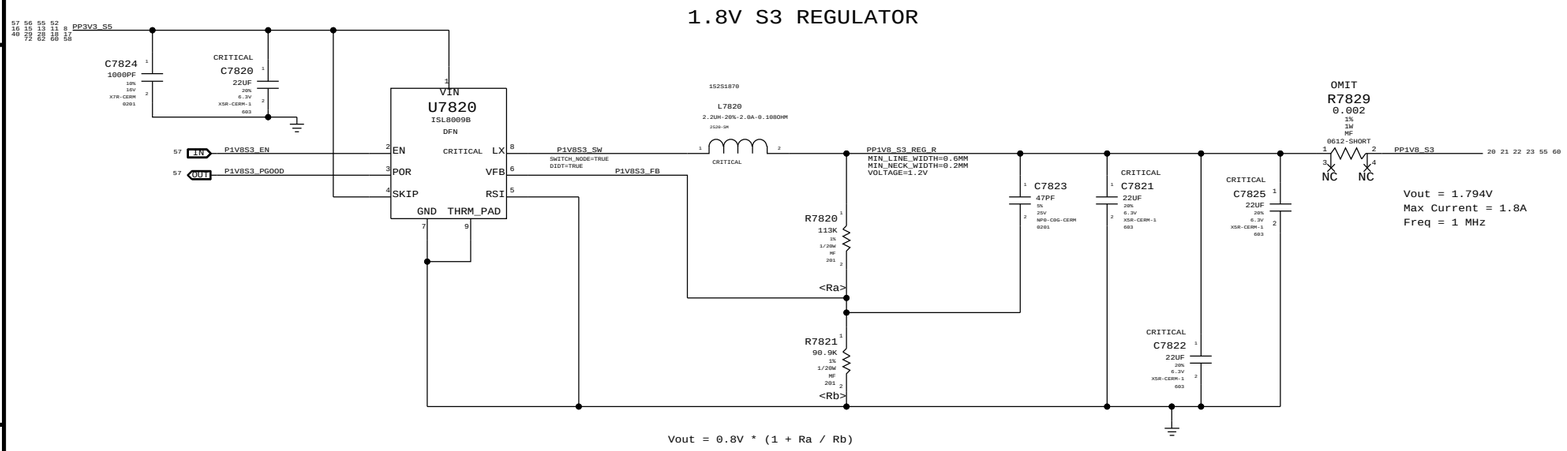
BRANCH: <BRANCH>

PAGE: 77 OF 120

SHEET: 54 OF 73

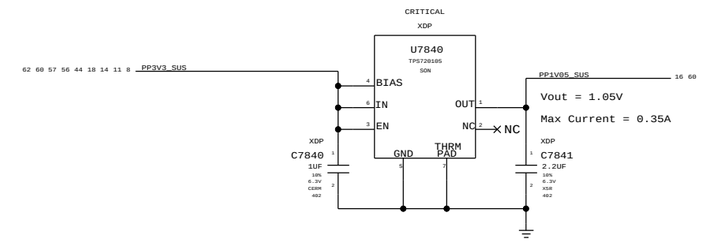
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.8V S3 REGULATOR

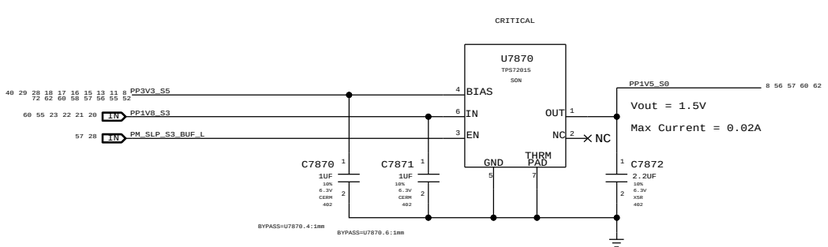


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

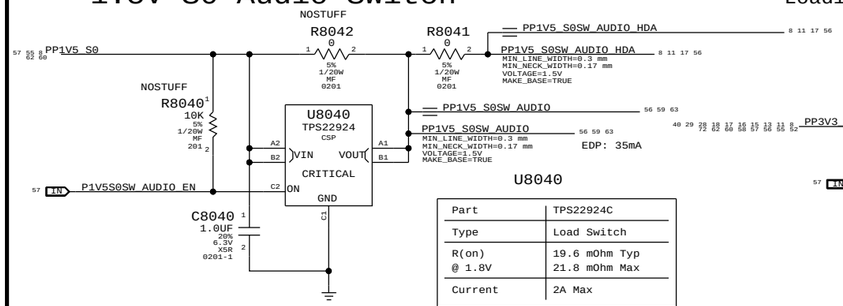
PAGE 78 OF 120

SHEET 55 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

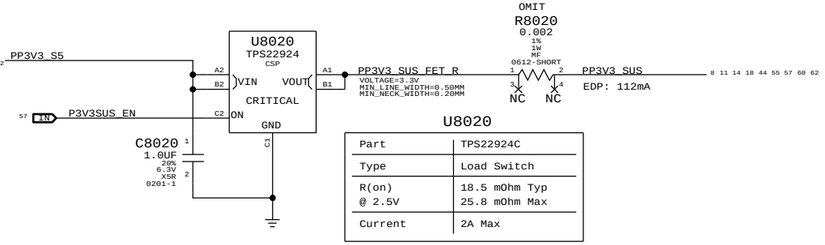
1.5V S0 Audio Switch



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

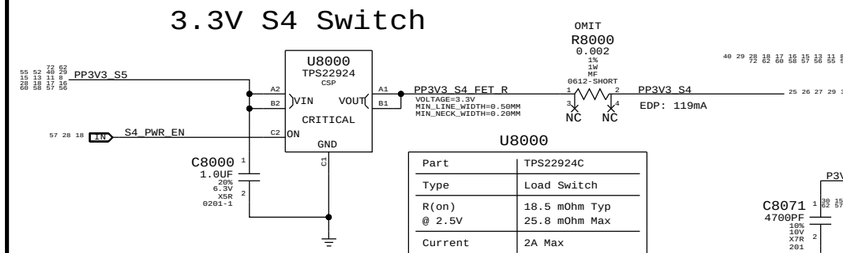
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

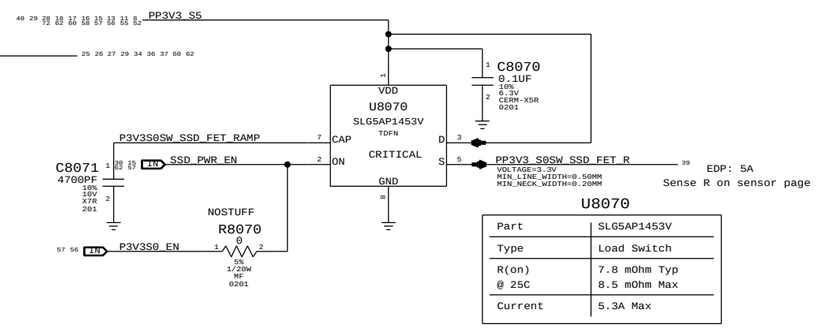
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

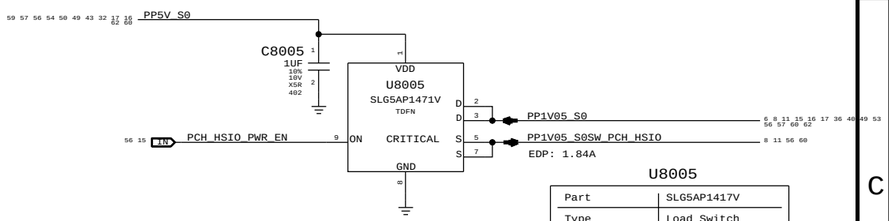
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

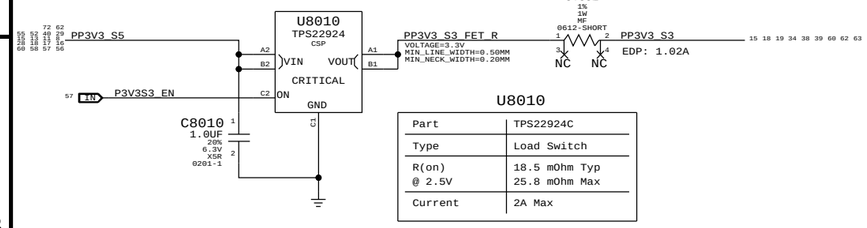


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

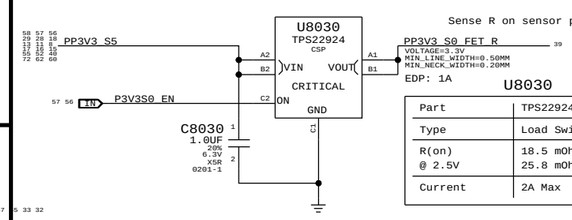
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

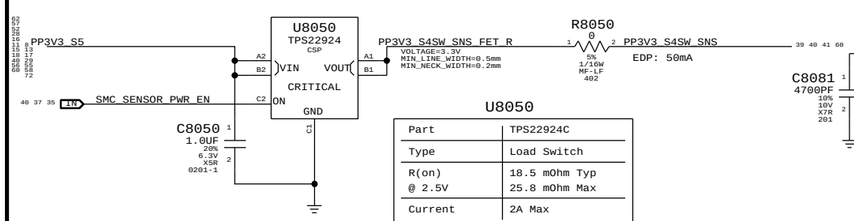
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

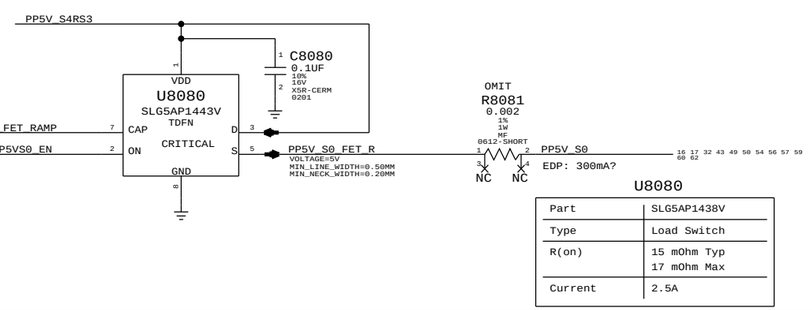
3.3V Sensor Switch



U8050

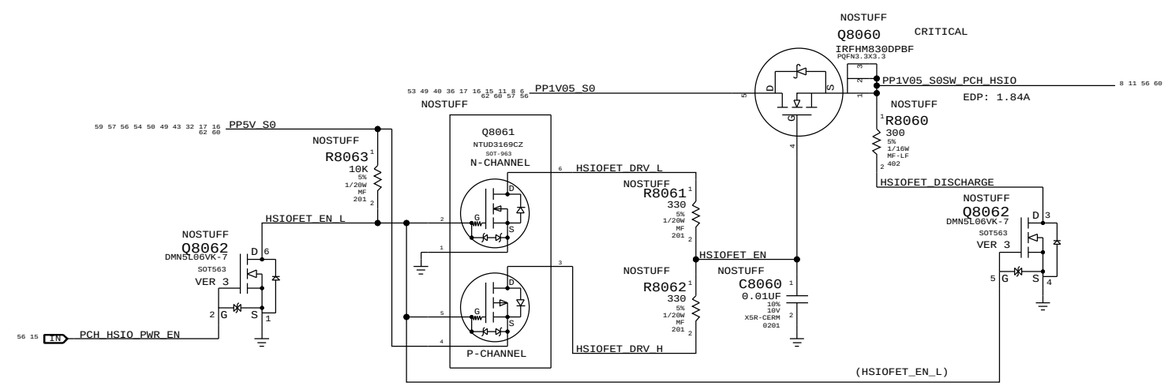
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

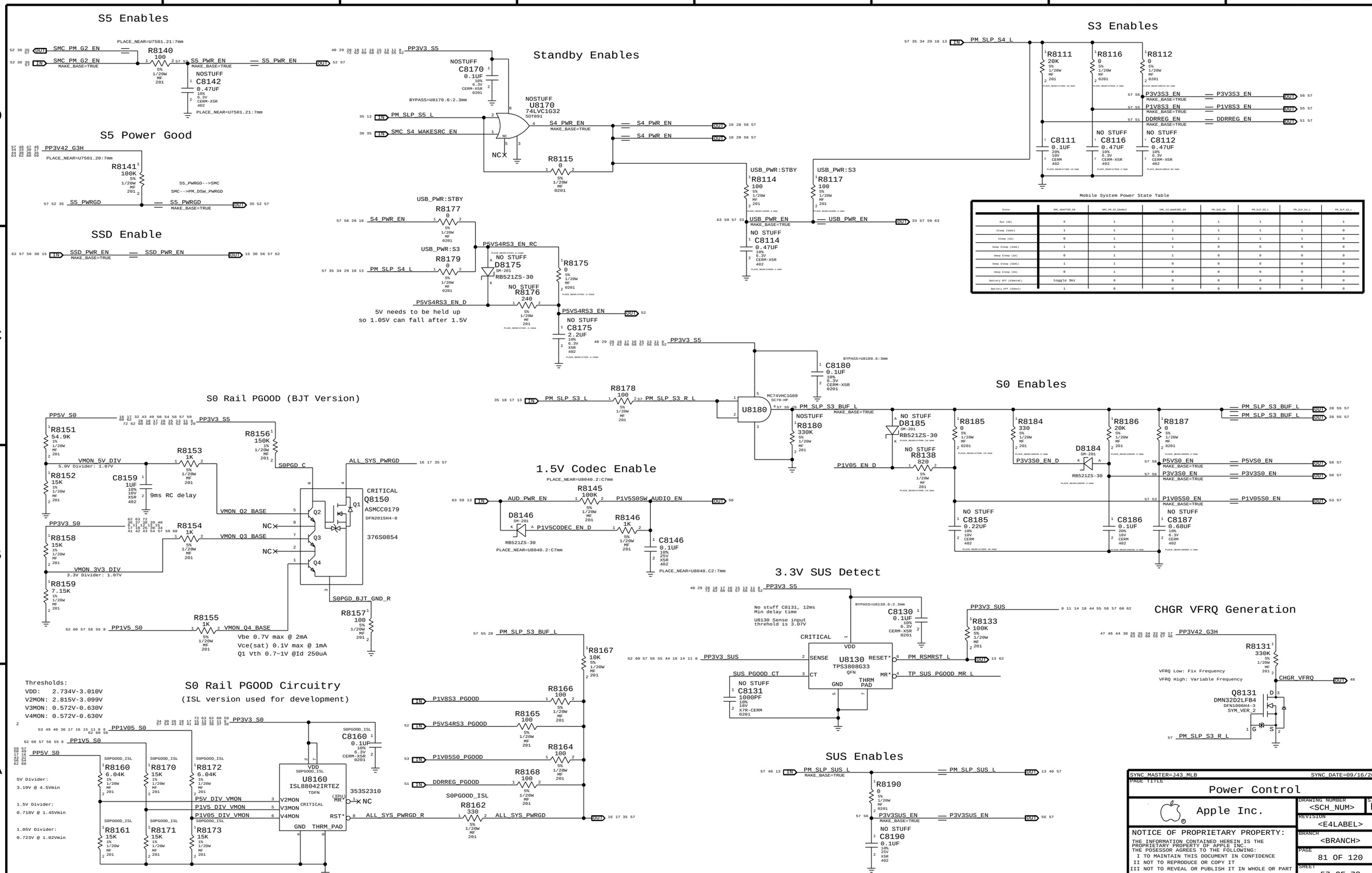
REVISION: <E4LABEL>

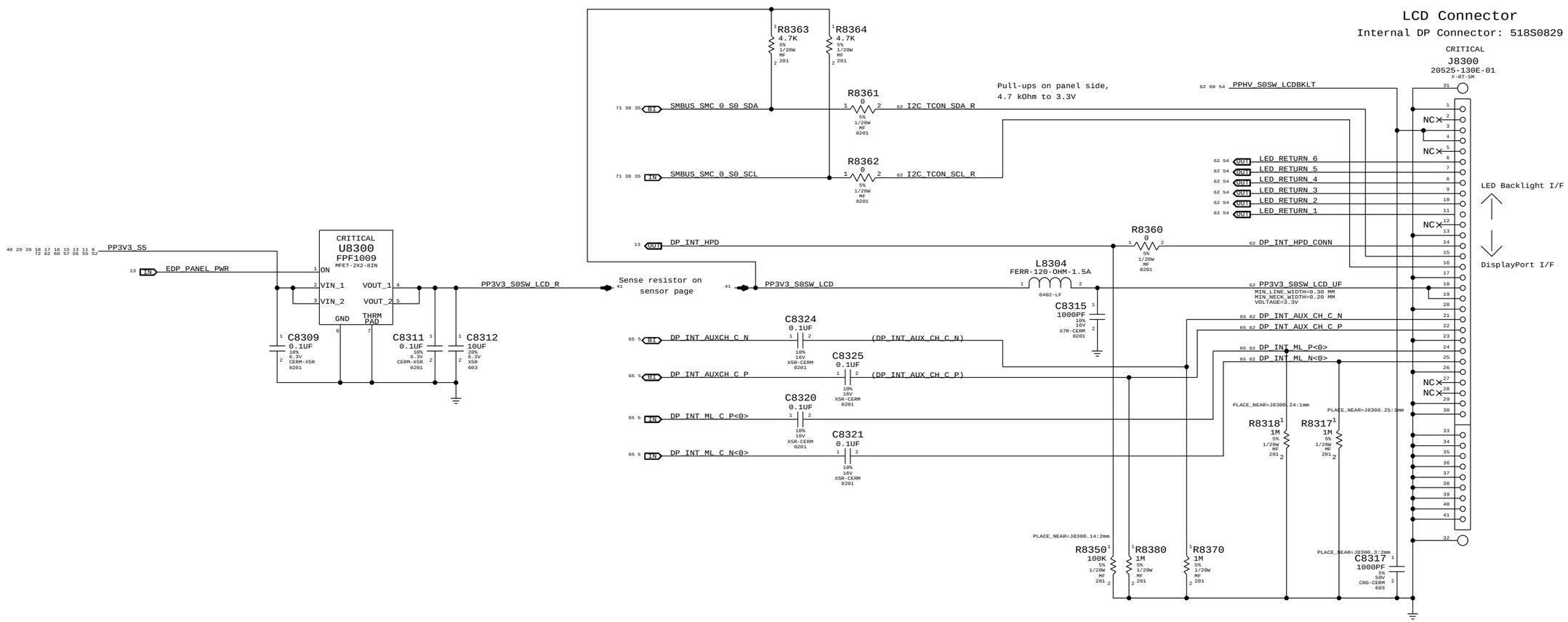
BRANCH: <BRANCH>

PAGE: 80 OF 120

SHEET: 56 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


S5 Enables
SMC_PM_G2_EN
R8140
100
S5_PWR_EN
C8142
0.47UF
S5 Power Good
PP3V42_G3H
R8141
100K
S5_PWRGD
SSD Enable
SSD_PWR_EN
Standby Enables
PP3V3_S5
C8170
0.1UF
U8170
74LVC1G32
PM_SLP_S5_L
SMC_S4_WAKESRC_EN
S4_PWR_EN
R8115
USB_PWR:STBY
R8114
USB_PWR:S3
R8117
USB_PWR_EN
C8114
0.47UF
R8177
R8179
PM_SLP_S4_L
D8175
RB521ZS-30
R8175
R8176
240
P5VS4RS3_EN_D
P5VS4RS3_EN_RC
P5VS4RS3_EN
C8175
2.2UF
5V needs to be held up
so 1.05V can fall after 1.5V
S3 Enables
PM_SLP_S4_L
R8111
20K
R8116
0
R8112
0
P3V3S3_EN
P1V8S3_EN
DDRREG_EN
C8111
0.1UF
C8116
0.47UF
C8112
0.47UF
Mobile System Power State Table
S0 Rail PGOOD (BJT Version)
PP5V_S0
R8151
54.9K
R8156
150K
R8153
1K
VMON_5V_DIV
5.0V Divider: 1.07V
R8152
15K
C8159
1UF
9ms RC delay
S0PGD_C
ALL_SYS_PWRGD
CRITICAL
Q8150
ASMCC0179
DFN2015H4-8
376S0854
Q1
Q2
Q3
Q4
VMON_Q2_BASE
VMON_Q3_BASE
R8154
1K
R8158
15K
VMON_3V3_DIV
3.3V Divider: 1.07V
R8159
7.15K
R8155
1K
VMON_Q4_BASE
S0PGD_BJT_GND_R
R8157
100
Vbe 0.7V max @ 2mA
Vce(sat) 0.1V max @ 1mA
Q1 Vth 0.7~1V @Id 250uA
S0 Rail PGOOD Circuitry
(ISL version used for development)
Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V
5V Divider:
3.19V @ 4.5Vmin
1.5V Divider:
0.718V @ 1.45Vmin
1.05V Divider:
0.723V @ 1.02Vmin
R8160
6.04K
R8170
15K
R8172
6.04K
R8161
15K
R8171
15K
R8173
15K
U8160
ISL88042IRTEZ
TDFN
V2MON
V3MON
V4MON
GND
THRM_PAD
P5V_DIV_VMON
P1V5_DIV_VMON
P1V05_DIV_VMON
S0PGOOD_ISL
C8160
0.1UF
353S2310
ALL_SYS_PWRGD_R
R8167
10K
R8166
100
R8165
100
R8164
100
R8168
100
R8162
330
1.5V Codec Enable
AUD_PWR_EN
R8145
100K
P1V5S0SW_AUDIO_EN
D8146
RB521ZS-30
P1V5CODEC_EN_D
R8146
1K
C8146
0.1UF
PLACE_NEAR=U8040.C2:7mm
3.3V SUS Detect
No stuff C8131, 12ms
Min delay time
U8130 Sense input
threhold is 3.07V
C8130
0.1UF
PP3V3_SUS
R8133
100K
U8130
TPS3808G33
SENSE
RESET*
MR*
CT
GND
THRM PAD
PM_RSMRST_L
TP_SUS_PGOOD_MR_L
SUS_PGOOD_CT
C8131
1000PF
SUS Enables
PM_SLP_SUS_L
R8190
0
P3V3SUS_EN
C8190
0.1UF
S0 Enables
PM_SLP_S3_R_L
PM_SLP_S3_L
R8178
100
U8180
MC74VHC1G08
PM_SLP_S3_BUF_L
C8180
0.1UF
R8180
330K
D8185
RB521ZS-30
R8138
820
P1V05_EN_D
R8185
0
R8184
330
P3V3S0_EN_D
D8184
RB521ZS-30
R8186
20K
R8187
0
P5VS0_EN
P3V3S0_EN
P1V05S0_EN
C8185
0.22UF
C8186
0.1UF
C8187
0.68UF
CHGR VFRQ Generation
PP3V42_G3H
R8131
330K
VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency
CHGR_VFRQ
Q8131
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
PM_SLP_SUS_L
P3V3SUS_EN
C8190
0.1UF
SYNC_MASTER=J43_MLB
SYNC_DATE=09/16/2013
PAGE TITLE
Power Control
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
81 OF 120
SHEET
57 OF 73
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J43_MLB SYNC_DATE=09/11/2012

PAGE TITLE

Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

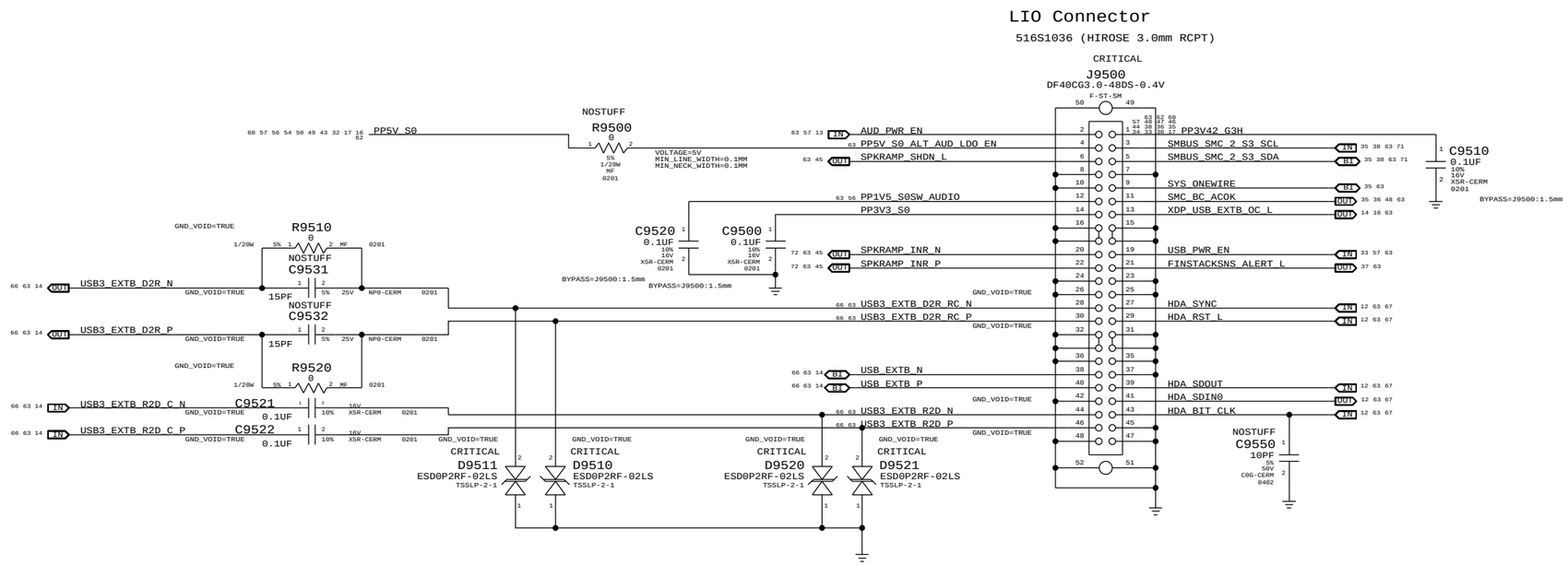
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 83 OF 120

SHEET 58 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=CLEAN J41 SYNC DATE=11/13/2012

PAGE TITLE

LIO Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 95 OF 120

SHEET 59 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

"G3Hot" (Always-Present) Rails

PPBUS_G3H → PPBUS_G3H (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.6V, MAKE_BASE=TRUE)
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H

PPBUS_S5_HS_COMPUTING_ISNS → PPBUS_S5_HS_COMPUTING_ISNS (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.6V, MAKE_BASE=TRUE)
- PPBUS_S5_HS_COMPUTING_ISNS
- PPBUS_S5_HS_COMPUTING_ISNS
- PPBUS_S5_HS_COMPUTING_ISNS

PPBUS_S5_HS_OTHER_ISNS → PPBUS_S5_HS_OTHER_ISNS (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.6V, MAKE_BASE=TRUE)
- PPBUS_S5_HS_OTHER_ISNS

PPDCIN_G3H_ISOL → PPDCIN_G3H_ISOL (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=18.5V, MAKE_BASE=TRUE)
- PPDCIN_G3H_ISOL
- PPDCIN_G3H_ISOL

PPDCIN_G3H → PPDCIN_G3H (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=18.5V, MAKE_BASE=TRUE)
- PPDCIN_G3H

PP3V42_G3H → PP3V42_G3H (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE)
- PP3V42_G3H
- PP3V42_G3H
- PP3V42_G3H

LPDDR3 Command/Address

	7	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	20 24 68
	7	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	20 24 68
	7	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	20 24 68
	7	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	20 24 68
	7	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	20 24 68
	7	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	20 24 68
68 61 24 20	7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	7 20 24 61 68
	7	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	20 24 68
	7	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	20 24 68
	7	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	20 24 68
	7	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	21 24 68
	7	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	21 24 68
	7	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	21 24 68
	7	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	21 24 68
	7	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	21 24 68
	7	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	21 24 68
68 61 24 21	7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	7 21 24 61 68
	7	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	21 24 68
	7	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	21 24 68
	7	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	21 24 68
68 61 24 21 20	7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	7 20 21 24 61 68
61	7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	7 61
61	7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	7 61
	7	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	22 24 68
	7	=MEM_B_A<9>	TRUE	MEM_B_CAA<1>	22 24 68
	7	=MEM_B_A<6>	TRUE	MEM_B_CAA<2>	22 24 68
	7	=MEM_B_A<8>	TRUE	MEM_B_CAA<3>	22 24 68
	7	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>	22 24 68
	7	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>	22 24 68
68 61 24 22	7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	7 22 24 61 68
	7	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	22 24 68
	7	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>	22 24 68
	7	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>	22 24 68
	7	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	23 24 68
	7	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>	23 24 68
	7	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	23 24 68
	7	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	23 24 68
	7	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>	23 24 68
	7	=MEM_B_A<2>	TRUE	MEM_B_CAB<5>	23 24 68
68 61 24 23	7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	7 23 24 61 68
	7	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	23 24 68
	7	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>	23 24 68
	7	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>	23 24 68
68 61 24 23 22	7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	7 22 23 24 61 68
61	7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	7 61
61	7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	7 61

Memory Bit/Byte Swizzle

	20	=MEM_A_DQ<0>	TRUE	MEM_A_DQ<9>	7 68
	20	=MEM_A_DQ<1>	TRUE	MEM_A_DQ<12>	7 68
	20	=MEM_A_DQ<2>	TRUE	MEM_A_DQ<10>	7 68
	20	=MEM_A_DQ<3>	TRUE	MEM_A_DQ<11>	7 68
	20	=MEM_A_DQ<4>	TRUE	MEM_A_DQ<8>	7 68
	20	=MEM_A_DQ<5>	TRUE	MEM_A_DQ<13>	7 68
	20	=MEM_A_DQ<6>	TRUE	MEM_A_DQ<14>	7 68
	20	=MEM_A_DQ<7>	TRUE	MEM_A_DQ<15>	7 68
	20	=MEM_A_DQ<8>	TRUE	MEM_A_DQ<0>	7 68
	20	=MEM_A_DQ<9>	TRUE	MEM_A_DQ<1>	7 68
	20	=MEM_A_DQ<10>	TRUE	MEM_A_DQ<2>	7 68
	20	=MEM_A_DQ<11>	TRUE	MEM_A_DQ<7>	7 68
	20	=MEM_A_DQ<12>	TRUE	MEM_A_DQ<4>	7 68
	20	=MEM_A_DQ<13>	TRUE	MEM_A_DQ<5>	7 68
	20	=MEM_A_DQ<14>	TRUE	MEM_A_DQ<3>	7 68
	20	=MEM_A_DQ<15>	TRUE	MEM_A_DQ<6>	7 68
	20	=MEM_A_DQ<16>	TRUE	MEM_A_DQ<29>	7 68
	20	=MEM_A_DQ<17>	TRUE	MEM_A_DQ<28>	7 68
	20	=MEM_A_DQ<18>	TRUE	MEM_A_DQ<27>	7 68
	20	=MEM_A_DQ<19>	TRUE	MEM_A_DQ<31>	7 68
	20	=MEM_A_DQ<20>	TRUE	MEM_A_DQ<24>	7 68
	20	=MEM_A_DQ<21>	TRUE	MEM_A_DQ<25>	7 68
	20	=MEM_A_DQ<22>	TRUE	MEM_A_DQ<26>	7 68
	20	=MEM_A_DQ<23>	TRUE	MEM_A_DQ<30>	7 68
	20	=MEM_A_DQ<24>	TRUE	MEM_A_DQ<18>	7 68
	20	=MEM_A_DQ<25>	TRUE	MEM_A_DQ<21>	7 68
	20	=MEM_A_DQ<26>	TRUE	MEM_A_DQ<16>	7 68
	20	=MEM_A_DQ<27>	TRUE	MEM_A_DQ<23>	7 68
	20	=MEM_A_DQ<28>	TRUE	MEM_A_DQ<20>	7 68
	20	=MEM_A_DQ<29>	TRUE	MEM_A_DQ<19>	7 68
	20	=MEM_A_DQ<30>	TRUE	MEM_A_DQ<22>	7 68
	20	=MEM_A_DQ<31>	TRUE	MEM_A_DQ<17>	7 68
	21	=MEM_A_DQ<32>	TRUE	MEM_A_DQ<41>	7 68
	21	=MEM_A_DQ<33>	TRUE	MEM_A_DQ<44>	7 68
	21	=MEM_A_DQ<34>	TRUE	MEM_A_DQ<46>	7 68
	21	=MEM_A_DQ<35>	TRUE	MEM_A_DQ<47>	7 68
	21	=MEM_A_DQ<36>	TRUE	MEM_A_DQ<40>	7 68
	21	=MEM_A_DQ<37>	TRUE	MEM_A_DQ<45>	7 68
	21	=MEM_A_DQ<38>	TRUE	MEM_A_DQ<42>	7 68
	21	=MEM_A_DQ<39>	TRUE	MEM_A_DQ<43>	7 68
	21	=MEM_A_DQ<40>	TRUE	MEM_A_DQ<36>	7 68
	21	=MEM_A_DQ<41>	TRUE	MEM_A_DQ<37>	7 68
	21	=MEM_A_DQ<42>	TRUE	MEM_A_DQ<34>	7 68
	21	=MEM_A_DQ<43>	TRUE	MEM_A_DQ<39>	7 68
68 61 21	7	MEM_A_DQ<32>	TRUE	MEM_A_DQ<32>	7 21 61 68
	21	=MEM_A_DQ<45>	TRUE	MEM_A_DQ<33>	7 68
	21	=MEM_A_DQ<46>	TRUE	MEM_A_DQ<35>	7 68
	21	=MEM_A_DQ<47>	TRUE	MEM_A_DQ<38>	7 68
	21	=MEM_A_DQ<48>	TRUE	MEM_A_DQ<52>	7 68
	21	=MEM_A_DQ<49>	TRUE	MEM_A_DQ<51>	7 68
	21	=MEM_A_DQ<50>	TRUE	MEM_A_DQ<48>	7 68
	21	=MEM_A_DQ<51>	TRUE	MEM_A_DQ<49>	7 68
	21	=MEM_A_DQ<52>	TRUE	MEM_A_DQ<53>	7 68
	21	=MEM_A_DQ<53>	TRUE	MEM_A_DQ<50>	7 68
	21	=MEM_A_DQ<54>	TRUE	MEM_A_DQ<54>	7 68
	21	=MEM_A_DQ<55>	TRUE	MEM_A_DQ<55>	7 68
	21	=MEM_A_DQ<56>	TRUE	MEM_A_DQ<58>	7 68
	21	=MEM_A_DQ<57>	TRUE	MEM_A_DQ<62>	7 68
	21	=MEM_A_DQ<58>	TRUE	MEM_A_DQ<60>	7 68
	21	=MEM_A_DQ<59>	TRUE	MEM_A_DQ<61>	7 68
	21	=MEM_A_DQ<60>	TRUE	MEM_A_DQ<59>	7 68
	21	=MEM_A_DQ<61>	TRUE	MEM_A_DQ<63>	7 68
	21	=MEM_A_DQ<62>	TRUE	MEM_A_DQ<57>	7 68
	21	=MEM_A_DQ<63>	TRUE	MEM_A_DQ<56>	7 68
	20	=MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<1>	7 68
	20	=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<1>	7 68
	20	=MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<0>	7 68
	20	=MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<0>	7 68
	20	=MEM_A_DQS_P<2>	TRUE	MEM_A_DQS_P<3>	7 68
	20	=MEM_A_DQS_N<2>	TRUE	MEM_A_DQS_N<3>	7 68
	20	=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<2>	7 68
	20	=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<2>	7 68
	21	=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<5>	7 68
	21	=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<5>	7 68
	21	=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<4>	7 68
	21	=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<4>	7 68
68 61 21	7	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	7 21 61 68
68 61 21	7	MEM_A_DQS_N<6>	TRUE		7 21 61 68
	21	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<7>	7 68
	21	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<7>	7 68

	22	=MEM_B_DQ<0>	TRUE	MEM_B_DQ<12>	7 68
	22	=MEM_B_DQ<1>	TRUE	MEM_B_DQ<9>	7 68
	22	=MEM_B_DQ<2>	TRUE	MEM_B_DQ<10>	7 68
	22	=MEM_B_DQ<3>	TRUE	MEM_B_DQ<11>	7 68
	22	=MEM_B_DQ<4>	TRUE	MEM_B_DQ<13>	7 68
	22	=MEM_B_DQ<5>	TRUE	MEM_B_DQ<8>	7 68
	22	=MEM_B_DQ<6>	TRUE	MEM_B_DQ<14>	7 68
	22	=MEM_B_DQ<7>	TRUE	MEM_B_DQ<15>	7 68
	22	=MEM_B_DQ<8>	TRUE	MEM_B_DQ<0>	7 68
	22	=MEM_B_DQ<9>	TRUE	MEM_B_DQ<1>	7 68
	22	=MEM_B_DQ<10>	TRUE	MEM_B_DQ<2>	7 68
	22	=MEM_B_DQ<11>	TRUE	MEM_B_DQ<7>	7 68
	22	=MEM_B_DQ<12>	TRUE	MEM_B_DQ<4>	7 68
	22	=MEM_B_DQ<13>	TRUE	MEM_B_DQ<5>	7 68
	22	=MEM_B_DQ<14>	TRUE	MEM_B_DQ<6>	7 68
	22	=MEM_B_DQ<15>	TRUE	MEM_B_DQ<3>	7 68
	22	=MEM_B_DQ<16>	TRUE	MEM_B_DQ<28>	7 68
	22	=MEM_B_DQ<17>	TRUE	MEM_B_DQ<29>	7 68
	22	=MEM_B_DQ<18>	TRUE	MEM_B_DQ<30>	7 68
	22	=MEM_B_DQ<19>	TRUE	MEM_B_DQ<27>	7 68
	22	=MEM_B_DQ<20>	TRUE	MEM_B_DQ<24>	7 68
	22	=MEM_B_DQ<21>	TRUE	MEM_B_DQ<25>	7 68
	22	=MEM_B_DQ<22>	TRUE	MEM_B_DQ<31>	7 68
	22	=MEM_B_DQ<23>	TRUE	MEM_B_DQ<26>	7 68
	22	=MEM_B_DQ<24>	TRUE	MEM_B_DQ<20>	7 68
	22	=MEM_B_DQ<25>	TRUE	MEM_B_DQ<16>	7 68
	22	=MEM_B_DQ<26>	TRUE	MEM_B_DQ<23>	7 68
	22	=MEM_B_DQ<27>	TRUE	MEM_B_DQ<22>	7 68
	22	=MEM_B_DQ<28>	TRUE	MEM_B_DQ<21>	7 68
	22	=MEM_B_DQ<29>	TRUE	MEM_B_DQ<17>	7 68
	22	=MEM_B_DQ<30>	TRUE	MEM_B_DQ<18>	7 68
	22	=MEM_B_DQ<31>	TRUE	MEM_B_DQ<19>	7 68
	23	=MEM_B_DQ<32>	TRUE	MEM_B_DQ<44>	7 68
	23	=MEM_B_DQ<33>	TRUE	MEM_B_DQ<41>	7 68
	23	=MEM_B_DQ<34>	TRUE	MEM_B_DQ<42>	7 68
	23	=MEM_B_DQ<35>	TRUE	MEM_B_DQ<43>	7 68
	23	=MEM_B_DQ<36>	TRUE	MEM_B_DQ<45>	7 68
	23	=MEM_B_DQ<37>	TRUE	MEM_B_DQ<40>	7 68
	23	=MEM_B_DQ<38>	TRUE	MEM_B_DQ<46>	7 68
	23	=MEM_B_DQ<39>	TRUE	MEM_B_DQ<47>	7 68
	23	=MEM_B_DQ<40>	TRUE	MEM_B_DQ<32>	7 68
68 61 23	7	MEM_B_DQ<33>	TRUE	MEM_B_DQ<33>	7 23 61 68
	23	=MEM_B_DQ<42>	TRUE	MEM_B_DQ<34>	7 68
	23	=MEM_B_DQ<43>	TRUE	MEM_B_DQ<39>	7 68
	23	=MEM_B_DQ<44>	TRUE	MEM_B_DQ<36>	7 68
	23	=MEM_B_DQ<45>	TRUE	MEM_B_DQ<37>	7 68
	23	=MEM_B_DQ<46>	TRUE	MEM_B_DQ<38>	7 68
	23	=MEM_B_DQ<47>	TRUE	MEM_B_DQ<35>	7 68
	23	=MEM_B_DQ<48>	TRUE	MEM_B_DQ<57>	7 68
	23	=MEM_B_DQ<49>	TRUE	MEM_B_DQ<56>	7 68
	23	=MEM_B_DQ<50>	TRUE	MEM_B_DQ<60>	7 68
	23	=MEM_B_DQ<51>	TRUE	MEM_B_DQ<59>	7 68
	23	=MEM_B_DQ<52>	TRUE	MEM_B_DQ<63>	7 68
	23	=MEM_B_DQ<53>	TRUE	MEM_B_DQ<62>	7 68
	23	=MEM_B_DQ<54>	TRUE	MEM_B_DQ<58>	7 68
	23	=MEM_B_DQ<55>	TRUE	MEM_B_DQ<61>	7 68
	23	=MEM_B_DQ<56>	TRUE	MEM_B_DQ<49>	7 68
	23	=MEM_B_DQ<57>	TRUE	MEM_B_DQ<51>	7 68
	23	=MEM_B_DQ<58>	TRUE	MEM_B_DQ<48>	7 68
	23	=MEM_B_DQ<59>	TRUE	MEM_B_DQ<53>	7 68
	23	=MEM_B_DQ<60>	TRUE	MEM_B_DQ<52>	7 68
	23	=MEM_B_DQ<61>	TRUE	MEM_B_DQ<55>	7 68
	23	=MEM_B_DQ<62>	TRUE	MEM_B_DQ<50>	7 68
	23	=MEM_B_DQ<63>	TRUE	MEM_B_DQ<54>	7 68
	22	=MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<1>	7 68
	22	=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<1>	7 68
	22	=MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<0>	7 68
	22	=MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<0>	7 68
	22	=MEM_B_DQS_P<2>	TRUE	MEM_B_DQS_P<3>	7 68
	22	=MEM_B_DQS_N<2>	TRUE	MEM_B_DQS_N<3>	7 68
	22	=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<2>	7 68
	22	=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<2>	7 68
	23	=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<5>	7 68
	23	=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<5>	7 68
	23	=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<4>	7 68
	23	=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<4>	7 68
	23	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<7>	7 68
	23	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<7>	7 68
68 61 23	7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	7 23 61 68
68 61 23	7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	7 23 61 68

MEM_A_DQS_N<6>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Signal Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 102 OF 120

SHEET 61 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Functional Test Points

J3501: AirPort / BT Connector

FUNC_TEST		
TRUE	PP3V3_WLAN (Need 6 TPs)	29 35 36 37 39
TRUE	WIFI_EVENT_L	29 35 36
TRUE	PCIE_AP_R2D_N	29 67
TRUE	PCIE_AP_R2D_P	29 67
TRUE	PCIE_CLK100M_AP_N	12 29 67
TRUE	PCIE_CLK100M_AP_P	12 29 67
TRUE	PCIE_AP_D2R_P	14 29 67
TRUE	PCIE_AP_D2R_N	14 29 67
TRUE	PCIE_WAKE_L	13 29 31
TRUE	AP_RESET_CONN_L	29
TRUE	AP_CLKREQ_Q_L	29
TRUE	USB_BT_CONN_P	29 66
TRUE	USB_BT_CONN_N	29 66
TRUE	PP3V3_S4	25 26 27 29 34 36 37 56 60 62

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC_TEST		
TRUE	PP3V3_S0SW_SSD_FLT (Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>	30 65
TRUE	PCIE_SSD_R2D_P<3..0>	30 65
TRUE	PP3V3_S0	40 41 42 43 54 57 59
TRUE	SSD_RESET_CONN_L	40 41 42 43 15 17 48 26 30 34 36 37 38 39 60 62 63 72 30
TRUE	SSD_CLKREQ_CONN_L	30
TRUE	SMC_OOB1_R2D_CONN_L	30
TRUE	SMC_OOB1_D2R_CONN_L	30
TRUE	SSD_PCIE_SEL_L	30
TRUE	SSD_SR_EN_L	15 30
TRUE	SMC_PWRFAIL_WARN_L	30 35
TRUE	SSD_PWR_EN	15 30 56 57
TRUE	PCIE_SSD_D2R_N<3..0>	12 30 65
TRUE	PCIE_SSD_D2R_P<3..0>	12 30 65
TRUE	PCIE_CLK100M_SSD_N	12 30 65
TRUE	PCIE_CLK100M_SSD_P	12 30 65

(Need to add 6 GND TPs)

J4002: Camera Connector

FUNC_TEST		
TRUE	MIPI_CLK_CONN_N	32 70
TRUE	MIPI_CLK_CONN_P	32 70
TRUE	CAM_SENSOR_WAKE_L_CONN	32
TRUE	MIPI_DATA_CONN_N	32 70
TRUE	MIPI_DATA_CONN_P	32 70
TRUE	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 67 71
TRUE	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 67 71
TRUE	I2C_CAM_SCK	31 32
TRUE	I2C_CAM_SDA	31 32
TRUE	PP5V_S3RS0_ALSCAM_F (Need TBD TPs)	32

(Need to add TBD GND TPs)

J6100: LPC+SPI Connector

FUNC_TEST		
TRUE	SPI_ALT_IO3_HOLD_L	44
TRUE	SPI_ALT_IO2_WP_L	44
TRUE	LPC_AD<3..0>	14 35 67
TRUE	SPI_ALT_IO0_MOSI	44
TRUE	XDP_LPCPLUS_GPIO	15 16
TRUE	LPCPLUS_RESET_L	67
TRUE	SMC_TDO	35 36
TRUE	TP_SMC_TRST_L	
TRUE	TP_SMC_MD1	
TRUE	SMC_TX_L	35 36
TRUE	SPI_ALT_IO1_MISO	44
TRUE	LPC_FRAME_L	14 35 67
TRUE	SPIROM_USE_MLB	15 44
TRUE	PM_CLKRUN_L	13 35
TRUE	SPI_ALT_CLK	44
TRUE	SPI_ALT_CS_L	44
TRUE	LPC_SERIRQ	15 35
TRUE	LPC_PWRDWN_L	13 35
TRUE	SMC_TDI	35 36
TRUE	SMC_TCK	35 36 44
TRUE	SMC_RESET_L	35 36 44 48
TRUE	SMC_ROMBOOT	
TRUE	SMC_RX_L	35 36
TRUE	SMC_TMS	35 36 44

(Need to add 6 GND TPs)

J6000: Fan Connector

FUNC_TEST		
TRUE	PP5V_S0	16 17 32 43 49 50 54 56 57 59 60
TRUE	FAN_RT_TACH	43
TRUE	FAN_RT_PWM	43

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC_TEST		
TRUE	SMC_LID	34 35 36 46
TRUE	TPAD_SPI_MISO_R	34
TRUE	USB_TPAD_P	14 34 66
TRUE	USB_TPAD_N	14 34 66
TRUE	TPAD_SPI_CLK_R	34
TRUE	TPAD_WAKE_L	34
TRUE	TPAD_SPI_MOSI_R	34
TRUE	PP3V3_S4_IPD	34
TRUE	TPAD_SPI_CS_R_L	34
TRUE	TPAD_SPI_IF_EN_CONN	34
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN	34
TRUE	PP5V_S4_IPD	34
TRUE	TPAD_USB_IF_EN_CONN	34
TRUE	SMBUS_SMC_3_SDA	34 35 38 42 71
TRUE	SMBUS_SMC_3_SCL	34 35 38 42 71
TRUE	SMC_LSOC_RST_L	34 36
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMC_ONOFF_L	34 35 36

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC_TEST		
TRUE	PPDCIN_G3H (Need 4 TPs)	47 48 60 62
TRUE	PP5V_S4RS3 (Need 3 TPs)	32 33 45 47 52 53 56 60

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC_TEST		
TRUE	SPKRAMP_ROUT_P	45 72
TRUE	SPKRAMP_ROUT_N	45 72

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST		
TRUE	PPVBAT_G3H_CONN (Need 4 TPs)	46 48
TRUE	SMBUS_SMC_5_G3_SCL	35 38 46 48 71
TRUE	SMBUS_SMC_5_G3_SDA	35 38 46 48 71
TRUE	SYS_DETECT_L	46

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC_TEST		
TRUE	PPHV_S0SW_LCDBKLT (Need 2 TPs)	54 58 60
TRUE	LED_RETURN_6	54 58
TRUE	LED_RETURN_5	54 58
TRUE	LED_RETURN_4	54 58
TRUE	LED_RETURN_3	54 58
TRUE	LED_RETURN_2	54 58
TRUE	LED_RETURN_1	54 58
TRUE	DP_INT_HPD_CONN	58
TRUE	I2C_TCON_SDA_R	58
TRUE	I2C_TCON_SCL_R	58
TRUE	PP3V3_S0SW_LCD_UF (Need 2 TPs)	58
TRUE	DP_INT_AUX_CH_C_N	58 65
TRUE	DP_INT_AUX_CH_C_P	58 65
TRUE	DP_INT_ML_P<0>	58 65
TRUE	DP_INT_ML_N<0>	58 65

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC_TEST		
TRUE	KBDLED_ANODE	54
TRUE	KBDLED_FB	54

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 16 65
TRUE	XDP_PCH_TCK	12 16 67
TRUE	XDP_CPU_TDI	6 16 65
TRUE	XDP_CPU_TDO	6 16 65
TRUE	XDP_CPUPCH_TRST_L	6 12 16 65
TRUE	XDP_CPU_TMS	6 16 65
TRUE	XDP_PCH_TMS	12 16 67
TRUE	XDP_PCH_TDI	12 16 67
TRUE	XDP_PCH_TDO	12 16 67
TRUE	XDP_CPU_PREQ_L	6 16 65
TRUE	XDP_CPU_PRDY_L	6 16 65
TRUE	XDP_CPU_VCCST_PWRGD	16
TRUE	PM_RSMRST_L	13 57
TRUE	XDP_SYS_PWROK	16
TRUE	PM_SYSRST_L	13 17 35
TRUE	CPU_CFG<3>	6 16 65
TRUE	PP1V05_S0	6 9 11 15 16 17 36 40 49 53 56 57 60 62

(Need to add 2 GND TPs)

TRUE	GND	

Misc Voltages & Control Signals

FUNC_TEST		
TRUE	PPBUS_G3H	27 39 40 47 48 54 60
TRUE	PPVIN_S4SW_TBTBST_FET	27 60
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	39 49 50 51 53 60
TRUE	PPDCIN_G3H	47 48 60 62
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	PPVRTC_G3H	8 12 13 17 60
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 72
TRUE	PP3V3_SUS	8 11 14 18 44 55 56 57 60
TRUE	PP3V3_S3	15 18 19 34 38 39 56 60 63
TRUE	PP3V3_S0	60 62 63 72 8 11 12 13 14 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	PP3V3_S0SW_SSD	30 39 60
TRUE	PP1V5_S0	8 55 56 57 60
TRUE	PP1V05_S0	6 8 11 15 16 17 36 40 49 53 56 57 60 62
TRUE	PP15V_TBT	27 28 60
TRUE	PP3V3_TBTLC	17 18 25 26 60
TRUE	PP1V05_TBT	26
TRUE	PPVCC_S0_CPU	8 10 40 50 60
TRUE	PP1V05_TBTCIO	26 60
TRUE	PPBUS_S5_HS_OTHER_ISNS	39 52 60
TRUE	PPDCIN_G3H_ISOL	40 47 48 60
TRUE	PP3V3_S4	25 26 27 29 34 36 37 56 60 62

(Need to add 27 GND TPs)

NO_TEST Nets

		NO_TEST	MAKE_BASE			
62	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	62	CPU/PCH
62	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	62	CPU/PCH
62 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 62	CPU/PCH
62 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 62	CPU/PCH
62 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 62	CPU/PCH
62 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 62	CPU/PCH
62 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 62	CPU/PCH
62 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 62	CPU/PCH
62 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 62	CPU/PCH
62 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 62	CPU/PCH
62 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 62	CPU/PCH
62 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 62	CPU/PCH
62 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 62	CPU/PCH
62 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 62	CPU/PCH
65	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5	
65	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5	
62 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 62	
62 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 62	
62 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 62	
62 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 62	
62 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 62	
62 35	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	35 62	SMC
62	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	62	SMC
62	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	62	SMC
62	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	62	SMC
62 35	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	35 62	SMC
62 35	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	35 62	SMC
62 35	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	35 62	SMC
62 35	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	35 62	SMC
62 35	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	35 62	SMC
62	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	62	SMC
62	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	62	SMC
62	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	62	SMC
62 35	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	35 62	SMC
62 35	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	35 62	SMC
62 35	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	35 62	SMC
62 35	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	35 62	SMC
62 35	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	35 62	SMC
69	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25	TBT
69	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25	TBT
69	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25	TBT
69	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25	TBT
62 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 62	TBT
69 62	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	62 69	TBT
69 62	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	62 69	TBT
69 62 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 62 69	TBT
69 62 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 62 69	TBT
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>		TBT
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>		TBT
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>		TBT
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>		TBT
62 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 62	TBT
62 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 62	TBT
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>		TBT
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>		TBT
62 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 62	TBT
62 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 62	TBT

Unused nets with offpage

(Nets with offpages not used on this project)

PCH_BT_UART_D2R	15
PCH_BT_UART_R2D	15
PCH_BT_UART_RTS_L	15
PCH_BT_UART_CTS_L	15
AUD_SPI_CS_L	15
AUD_SPI_CLK	15
AUD_SPI_MISO	15
AUD_SPI_MOSI	15
HDMITBTMUX_LATCH	13
HDD_PWR_EN	15
WOL_EN	14
BT_PWRRST_L	15
HDMITBTMUX_FLAG	13
FW_PWR_EN	
FW_PME_L	
ENET_MEDIA_SENSE	15
LCD_PSR_EN	15
LCD_IRQ_L	15
ODD_PWR_EN_L	13
ENET_LOW_PWR	13
AUD_IP_PERIPHERAL_DET	
AUD_I2C_INT_L	
AP_PCIE_DEV_WAKE	13

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE

Func Test / No Test

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 104 OF 120

SHEET 62 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Functional Test Points

J9500: LIO Connector

FUNC_TEST			
TRUE	AUD_PWR_EN	13 57 59	
TRUE	PP5V_S0_ALT_AUD_LDO_EN	59	
TRUE	SPKRAMP_SHDN_L	45 59	
TRUE	PP1V5_S0SW_AUDIO	56 59	
TRUE	PP3V3_S0	60 62 72 5 11 12 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59	
TRUE	SPKRAMP_INR_N	45 59 72	
TRUE	SPKRAMP_INR_P	45 59 72	
TRUE	USB3_EXTB_D2R_RC_N	59 63 66	
TRUE	USB3_EXTB_D2R_RC_P	59 63 66	
TRUE	USB_EXTB_N	14 59 66	
TRUE	USB_EXTB_P	14 59 66	
TRUE	USB3_EXTB_R2D_N	59 63 66	
TRUE	USB3_EXTB_R2D_P	59 63 66	
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63	
TRUE	SMBUS_SMC_2_S3_SCL	35 38 59 71	
TRUE	SMBUS_SMC_2_S3_SDA	35 38 59 71	
TRUE	SYS_ONEWIRE	35 59	
TRUE	SMC_BC_ACOK	35 36 48 59	
TRUE	XDP_USB_EXTB_OC_L	14 16 59	
TRUE	USB_PWR_EN	33 57 59	
TRUE	FINSTACKSNS_ALERT_L	37 59	
TRUE	HDA_SYNC	12 59 67	
TRUE	HDA_RST_L	12 59 67	
TRUE	HDA_SDOUT	12 59 67	
TRUE	HDA_SDIN0	12 59 67	
TRUE	HDA_BIT_CLK (Need to add 5 GND TPs)	12 59 67	

J6955: HALL EFFECT Connector

FUNC_TEST		
TRUE	SMC_LID_R	46
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63

Power Aliases

63 62 60 56 39 38 34 19 18 15 PP3V3_S3 — PP3V3_S3 15 18 19 34 38 39 56 60 62 63

NO_TEST Nets

		NO_TEST	MAKE_BASE			
66 63 14	NC_USB3RPCIE_SD_D2RP	TRUE	TRUE	NC_USB3RPCIE_SD_D2RP	14 63 66	
66 63 14	NC_USB3RPCIE_SD_D2RN	TRUE	TRUE	NC_USB3RPCIE_SD_D2RN	14 63 66	
66 63 14	NC_USB3RPCIE_SD_R2D_CP	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CP	14 63 66	CPU/PCH
66 63 14	NC_USB3RPCIE_SD_R2D_CN	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CN	14 63 66	
63 37 35	NC_SMC_ADC16	TRUE	TRUE	NC_SMC_ADC16	35 37 63	SMC

Bead Probes

66 59 14	USB3_EXTB_D2R_N	TP SM	BEAD-PROBE	BPA511
66 59 14	USB3_EXTB_D2R_P	TP SM	BEAD-PROBE	BPA510
66 63 59	USB3_EXTB_D2R_RC_N	TP SM	BEAD-PROBE	BPA520
66 63 59	USB3_EXTB_D2R_RC_P	TP SM	BEAD-PROBE	BPA521
66 59 14	USB3_EXTB_R2D_C_N	TP SM	BEAD-PROBE	BPA513
66 59 14	USB3_EXTB_R2D_C_P	TP SM	BEAD-PROBE	BPA512
66 63 59	USB3_EXTB_R2D_N	TP SM	BEAD-PROBE	BPA523
66 63 59	USB3_EXTB_R2D_P	TP SM	BEAD-PROBE	BPA522

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
XDP_SDCONN_STATE_CHANGE_L	15 16
SD_PWR_EN	15

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Project FCT/NC/Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 105 OF 120

SHEET 63 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

SYNC MASTER=J43_MLB SYNC DATE=10/24/2012

PAGE TITLE
PCB Rule Definitions

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 110 OF 120
SHEET 64 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted
back to TABLE_SPACING_RULE
once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 36
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_ITP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 16 62
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 16 62
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
	CPU_45S	CPU_ITP	CPU_CFG<11..0>	6 16 62
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 35
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 35 36 49
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_DMI	PM_THRMTRIP_L	15 36
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16 62
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16 62
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16 62
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16 62
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 12 16 62
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	
	CPU_45S	CPU_ITP	CPU_CFG<15..12>	6 16
(ESR_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 49
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 49
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 49
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 49
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 49
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 62
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 62
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 62
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 62
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	58 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	58 62
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 58 62
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 58
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 58
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

SYNC MASTER=J43_MLB SYNC DATE=09/21/2012

PAGE TITLE
CPU Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 111 OF 120
SHEET 65 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING			
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP		
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P		USB Hucopyb nets
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N		
USB_BT	USB_80D	USB	USB_BT_P	14 29	
USB_BT	USB_80D	USB	USB_BT_N	14 29	
	USB_80D	USB	USB_BT_CONN_P	29 62	
	USB_80D	USB	USB_BT_CONN_N	29 62	
	USB_80D	USB	USB_BT_WAKE_P		
	USB_80D	USB	USB_BT_WAKE_N		
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 34 62	
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 34 62	
	USB_80D	USB	USB_TPAD_CONN_P		
	USB_80D	USB	USB_TPAD_CONN_N		
	USB_80D	USB	TPAD_SPI_MOSI_USB_P		
	USB_80D	USB	TPAD_SPI_MISO_USB_N		
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P		
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N		
USB_SDCARD	USB_80D	USB	USB_SDCARD_P		
USB_SDCARD	USB_80D	USB	USB_SDCARD_N		
	SPI_45S	SPI	TPAD_SPI_MOSI	15 34	TP SPI nets
	SPI_45S	SPI	TPAD_SPI_MISO	15 34	
	SPI_45S	SPI	TPAD_SPI_CLK	15 34	
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 33	USB EXTA nets (Right USB port)
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 33	
	UART_45S	UART	SMC_DEBUGPRT_TX_L	33 35 36	
	UART_45S	UART	SMC_DEBUGPRT_RX_L	33 35 36	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	33	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	33	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	33	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	33	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 33	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 33	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	33	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	33	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P		
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N		
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P		
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N		
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 33	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 33	
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 59 63	USB EXTB nets (Left USB port)
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 59 63	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 59 63	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 59 63	
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	59 63	
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	59 63	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	59 63	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	59 63	
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 59 63	
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 59 63	
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RP	14 63	
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RN	14 63	
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CP	14 63	
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CN	14 63	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P		
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N		
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N		
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK		

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

PAGE TITLE: PCH Constraints 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 112 OF 120

SHEET: 66 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 35 62
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 35 62
	LPC_45S	LPC	LPCPLUS_RESET_L	62
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 35
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 19 38 54
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 19 38 54
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 38
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 38
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62 71
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62 71
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 59 63
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 59 63
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 59 63
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 59 63
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 59 63
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 36
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	35 36
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 44
	SPI_45S	SPI	SPI_CLK	44
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 44
	SPI_45S	SPI	SPI_MOSI	44
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 44
	SPI_45S	SPI	SPI_MISO_R	44
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 44
	SPI_45S	SPI	SPI_CS0_L	44
	SPI_45S	SPI	SPI_SMC_CLK	35 44
	SPI_45S	SPI	SPI_SMC_MOSI	35 44
	SPI_45S	SPI	SPI_SMC_MISO	35 44
	SPI_45S	SPI	SPI_SMC_CS_L	35 44
	SPI_45S	SPI	SPI_MLB_CLK	44
	SPI_45S	SPI	SPI_MLB_IO2_WP_L	44
	SPI_45S	SPI	SPI_MLB_IO3_HOLD_L	44
	SPI_45S	SPI	SPI_MLB_CS_L	44
	SPI_45S	SPI	SPI_IO<2>	14 44
	SPI_45S	SPI	SPI_IO2_R	44
	SPI_45S	SPI	SPI_IO<3>	14 44
	SPI_45S	SPI	SPI_IO3_R	44
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	29 62
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	29 62
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 29
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 29 62
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 29 62
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16 62
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16 62
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16 62
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16 62
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	31 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	31 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

PAGE TITLE

PCH Constraints 2

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 113 OF 120

SHEET 67 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 20 21 24 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	7 20 24 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	7 21 24 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 21 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 21 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 21 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 22 23 24 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	7 22 24 61
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	7 23 24 61
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 61
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 23 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 23 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 23 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 61
		MEM_PWR	PP1V2_S3	17 19 20 21 22 23 40 51 60
		MEM_PWR	PP0V6_S3_MEM_VREFCA_A	18 19 20 21
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_A	18 19 20 21
		MEM_PWR	PP0V6_S3_MEM_VREFCA_B	18 19 22 23
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_B	18 19 22 23

SYNC_MASTER=CHINMAY J41 SYNC_DATE=09/07/2012

PAGE TITLE

Memory Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 114 OF 120

SHEET 68 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	62
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	62
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2>	62
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2>	62
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	62
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP	25 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN	25 62
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CHINMAY_J41 SYNC_DATE=09/07/2012

PAGE TITLE

Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 115 OF 120

SHEET 69 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
1197	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
1192		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
1193	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
1194	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
1166	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
1168	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
1167	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
1165	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
1119	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
1147	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
1127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
1128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
1129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 62
1130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 62
1131	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
1132	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
1133		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 62
1134		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 62
1145			S2_MEM_PWR	PP1V35_CAM	31 32
1146			S2_MEM_PWR	PP0V675_CAM_VREF	31 32
1148			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
1149			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32

SYNC_MASTER=CHINMAY_J41 SYNC_DATE=09/07/2012

PAGE TITLE
Camera Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 116 OF 120

SHEET 70 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SCL	35 38 58
SMBUS_SMC_0_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SDA	35 38 58
SMBUS_SMC_1_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62 67
SMBUS_SMC_1_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62 67
SMBUS_SMC_2_S3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SCL	35 38 59 63
SMBUS_SMC_2_S3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SDA	35 38 59 63
SMBUS_SMC_3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_3_SCL	34 35 38 42 62
SMBUS_SMC_3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_3_SDA	34 35 38 42 62
SMBUS_SMC_5_G3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SCL	35 38 46 48 62
SMBUS_SMC_5_G3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SDA	35 38 46 48 62

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR			CHGR_CSI_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N	48
	2TO1_DIFFPAIR		CHGR_CSI_R_P	48
	2TO1_DIFFPAIR		CHGR_CSI_R_N	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N	48
	2TO1_DIFFPAIR		CHGR_CSO_R_P	41 48
	2TO1_DIFFPAIR		CHGR_CSO_R_N	41 48

SYNC_MASTER=CHINMAY_J41 SYNC_DATE=09/13/2012

PAGE TITLE
SMC Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 117 OF 120

SHEET 71 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.300 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	40 50
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R	40 41
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R	40 41
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P	40
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P	39
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P	40 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N	40 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P	41
DIFF SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	41 42
DIFF SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	41 42
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	45 59 63
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	45 59 63
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	45
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	45
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	45 62
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	45 62
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 49 52 60 62 63 55 56 57 58 60 62
		SB_POWER	PP3V3_S0	8 11 12 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
	GND		GND	

SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 118 OF 120

SHEET 72 OF 73

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Change List:
<rdar://component/508389> J41 HW EE Schematic | Proto 0
<rdar://component/512995> J41 HW EE Schematic | Pre Proto 1
<rdar://component/508412> J41 HW EE Schematic | Proto 1
<rdar://component/508413> J41 HW EE Schematic | EVT
<rdar://component/508414> J41 HW EE Schematic | DVT

Kismet:
afp://kismet.apple.com/Kismet-Projects/J41-J43

Useful Wiki Links:
Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:
<rdar://component/497591> MobileMac HW | Task
<rdar://component/497587> MobileMac HW | Schematic
<rdar://component/497585> MobileMac HW | New Bugs
<rdar://component/497588> MobileMac HW | Layout
<rdar://component/497590> MobileMac HW | Investigation
<rdar://component/497589> MobileMac HW | Architecture

Other Info:
Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE
Reference
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 120 OF 120
SHEET 73 OF 73

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED